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Design of Vedic- multiplier using GDI logic with 32nm technology

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Abstract: This proposed project presents a 4 bit Vedic multiplier. The performance of the system basically works better if the performance of the multiplier is good. In today's digital time, Multiplier is one which consumes power at the same time speed of multiplier is playing very important aspects in this. Multiplier Optimization for area and delay both will play an important role. GDI (Gate Diffusion Input) – a new technique of low power digital circuit design is described. This technique allows reducing power, area and delay, while maintaining low complexity of logic design. Performance comparison with GDI, CMOS and TG is presented, with respect to the power, delay and area showing advantage and drawbacks of GDI as compared to other methods. A variety of logic gates have been implemented in 32nm technology to compare the GDI technique with CMOS and TG. Vedic mathematics is an old mathematics which is more effective than other mathematic procedures. Vedic maths is utilized as a part of numerous applications, for example, hypothesis of numbers, compound duplications, squaring, cubing, square root and solid shape root and so on. Absolutely there are sixteen sutras and 14 sub-sutras in Vedic maths. Among those sutras, just 3 sutras and 2 sub sutras are utilized for augmentation. Multiplier is a very important part of microprocessor as multiplication is performed continuously in all calculative procedures. Adders such as Carry Look-ahead Adder(CLA), Carry Skip Adder(CSA) and Ripple Carry Adder(RCA) are also having a role in the selection of adder units in the multiplier. Here all the three adders are designed using GDI logic.

Keywords: *Gate Diffusion Input(GDI) Complementary Metal Oxide Semiconductor (CMOS), Transmission Gate (TG),Ripple Carry Adder(RCA), Carry Look Ahead(CLA), Carry Skip adder(CSA), Area, Delay.*

I. INTRODUCTION

Multipliers play an important role in today's digital signal processing and various other applications. In high performance systems uses addition and multiplication of two binary numbers is fundamental and most often used arithmetic operations. Statics shows that more than 70% instructions in microprocessor and most of DSP algorithms perform addition and multiplication. So, these operations overcome the execution time. That's why, there is need of high speed multiplier. The demand of high speed processing has been increasing as a result of expanding computer and signal processing applications. Low power consumption is also an important issue in multiplier design. To reduce significant power consumption it is good to reduce the number of operation thereby reducing dynamic power which is a major part of total power consumption so the need of high speed and low power multiplier has increased. Designer mainly concentrates on high speed and low power efficient circuit design. The aim of a good multiplier is to provide a physically packed together, high speed and low power consumption unit

A. Vedic Multiplier

Vedic mathematics is the name given to the ancient Indian system of mathematics that was rediscovered in early twentieth century. Vedic mathematics is mainly based on sixteen principles or word-formulae which are termed as Sutras. We discuss a possible application of Vedic mathematics to digital signal processing in the light of application of Vedic multiplication algorithm to digital multipliers. A simple digital multiplier (referred henceforth as Vedic multiplier) architecture based on the Urdhva Triyakbhyam (Vertically and Cross wise) Sutra is presented. This Sutra was traditionally used in ancient India for the multiplication of two decimal

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numbers in relatively less time. In this paper, after a gentle introduction of this Sutra, it is applied to the binary number system to make it useful in the digital hardware. The hardware architecture of the Vedic multiplier is presented and is shown to be very similar to that of the popular array multiplier. It is also equally likely that many such similar technical applications might come up from the storehouse of knowledge, Veda, if investigated properly.

Vedic mathematics is part of four Vedas (books of wisdom). It is part of Sthapatya Veda (book on civil engineering and architecture), which is an Upa-Veda (supplement) of Atharva Veda. It covers explanation of several modern mathematical terms including arithmetic, geometry (plane, co-ordinate), trigonometry, quadratic equations, factorization and even calculus. His Holiness Jagadguru Shankaracharya Bharati Krishna Teerthaji Maharaja (1884-1960) comprised all this work together and gave its mathematical explanation while discussing it for various applications. Swamhiji constructed 16 sutras (formulae) and 16 Upa sutras (sub formulae) after extensive research in Atharva Veda. The very word "Veda" has the derivational meaning i.e. the fountainhead and illimitable storehouse of all knowledge. Vedic mathematics is the name given to the ancient system of mathematics or, to be precise a unique technique of calculations based on simple rules and principles with which many mathematical problems can be solved, be it arithmetic, algebra, geometry or trigonometry. The system is based on 16 Vedic sutras or aphorisms, which are actually word formulae describing natural ways of solving a whole range of mathematical problems. The beauty of Vedic mathematics lies in the fact that it reduces the otherwise cumbersome-looking calculations in conventional mathematics to a very simple one. This is so because the Vedic formulae are claimed to be based on the natural principles on which the human mind works. This is a very interesting field and presents some effective algorithms which can be applied to various branches of engineering such as computing and digital signal processing.

Multiplication of two, 4 digit numbers with this method.

Ex: the product of 1111 and 1111 using Triyakbhyam (vertically and crosswise) is given below:

Method for calculating the 1 1 1 1 x 1 1 1 1

1 1 1 1

1 x 1 = 1

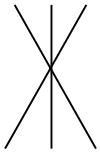
1 1 1 1

1 1 1 1

1 x 1+1 x 1 = 2

1 1 1 1

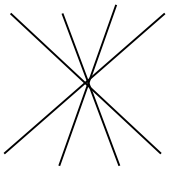
1 1 1 1



1 x 1+1 x 1+ 1 x 1 = 3

1 1 1 1

1 1 1 1



1 x 1+1 x 1+1 x 1+1 x 1 = 4

1 1 1 1

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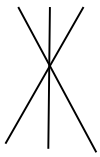
1 1 1 1



1 x 1+1 x 1+ 1 x 1 = 3

1 1 1 1

1 1 1 1

1 x 1+1 x 1 = 2

1 1 1 1

1 1 1 1

1 x 1 = 1

1 1 1 1

ANS for 1111 x 1111 = 1 2 3 4 3 2 1

This is the basic way for implementing 4 bit multiplication using Vedic (Urdhva Triyakbhyam sutra) but it is a complex way by increasing the bit size.

In another way, implementation of 4 bit multiplier is as follows:

First we have to implement 2 bit Vedic multiplier, by using those two bit multiplier we can design 4 bit multiplier as follows:

1 1

1 x 1 = 1

1 1

1 1

1 x 1+1 x 1 = 2

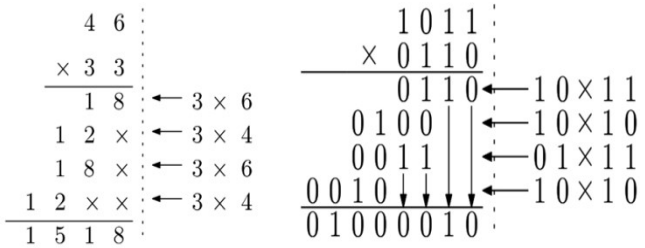
I 1

1 1

1 x 1 = 1

1 1

Answer for 2 bit multiplier is 121, by using 2 bit Example:



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By using adders, we get the final result.

```
  1   2   1
          2   4   2
      1   2   1
  ---------------------
  1   2   3   4   3   2   1
```

The dedicated multiplication circuit uses Full Adder's circuit to perform Carryout Multiplication. Hence the performance of multiplier also depends on the performance of the adder.

Ripple Carry Adder(RCA)

Multiple full adder circuits can be cascaded in parallel to add an N-bit number. For an N- bit parallel adder, there must be N number of full adder circuits. A ripple carry adder is a logic circuit in which the carry-out of each full adder is the carry in of the succeeding next most significant full adder. It is called a ripple carry adder because each carry bit gets rippled into the next stage. In a ripple carry adder the sum and carry out bits of any half adder stage is not valid until the carry in of that stage occurs. Propagation delays inside the logic circuitry is the reason behind this. Propagation delay is time elapsed between the application of an input and occurance of the corresponding output. Consider a NOT gate, When the input is "0" the output will be "1" and vice versa. The time taken for the NOT gate's output to become "0" after the application of logic "1" to the NOT gate's input is the propagation delay here. Similarly the carry propagation delay is the time elapsed between the application of the carry in signal and the occurance of the carry out (Cout) signal.

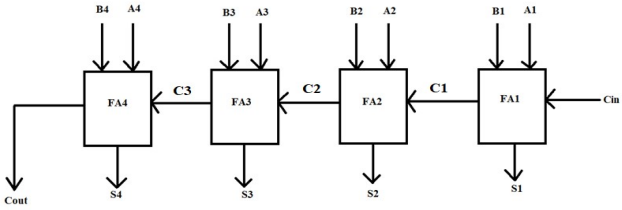

Fig. 1. 4-bit Ripple Carry Adder

Carry Look-ahead Adder(CLA)

A carry look-ahead adder reduces the propagation delay by introducing more complex hardware. In this design, the ripple carry design is suitably transformed such that the carry logic over fixed groups of bits of the adder is reduced to two-level logic. The carry out bit of the last adder doesn't wait the carry bits of previous adder. Here, all the carry bits of each adder are produced at the same time. Hence, the propagation delay reduces compared to Ripple Carry Adder.

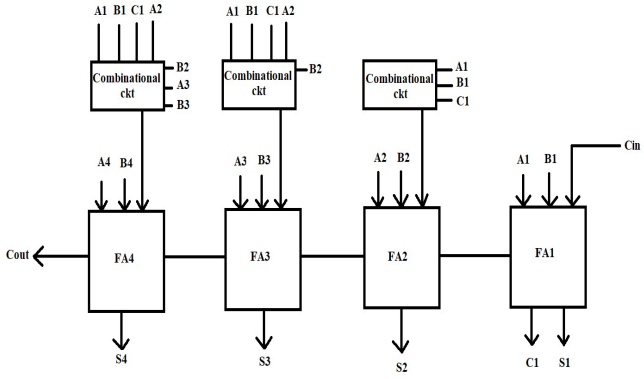

Fig. 2. 4-bit Carry Look-ahead Adder

Carry Skip Adder(CSA)

A Carry Skip adder comes under the category of digital adders. In this the logic AND gate is used for the every stage of adder to check whether the carry is present or not. If not the carry bit is directly fed to the last stage of adder. By this, the carry need not to propagate through all the stages of adder in every sequence of input. A carry-skip adder (also known as

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a carry-bypass adder) is an adder implementation that improves on the delay of a ripple-carry adder with little effort compared to other adders. The improvement of the worst-case delay is achieved by using several carry-skip adders to form a block-carry-skip adder.

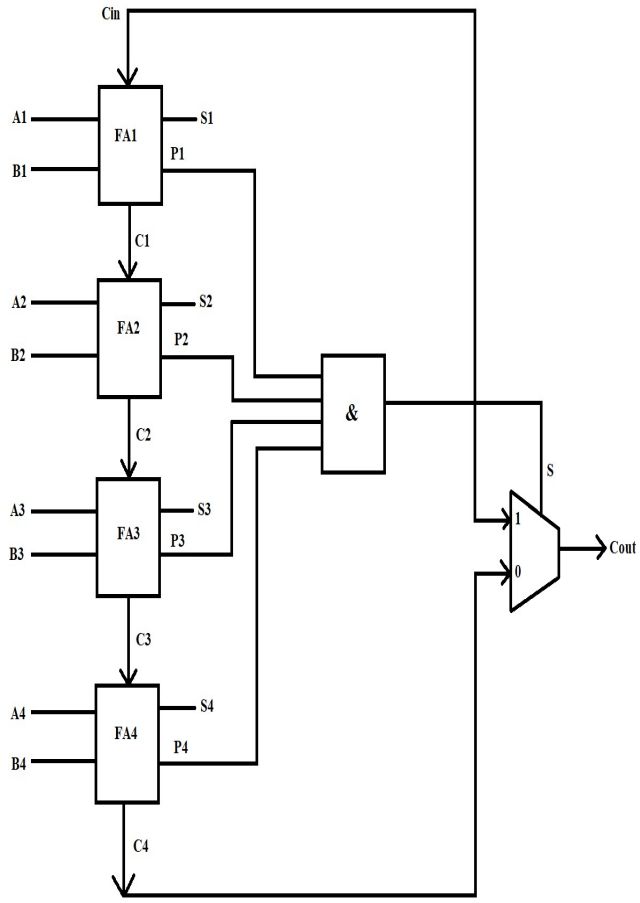

Fig. 3. 4-bit Carry Skip Adder

II . METHODOLOGY

A. Gate Diffusion Input(GDI) Logic:

GDI defines Gate Diffusion Input. Comparing to the structure of CMOS, GDI provides Drain and sources terminals also as input terminals. Due to this structure, we can design the structures using little number of transistors that's GDI implementation offers area efficiency comparing to other configurations. By this, we can reduce area and delay. Gate Diffusion Input (GDI) is a lowest power design technique which offers improved logic swing and less static power dissipation. Using this technique several logic functions can be implemented using less number of transistor counts. This method is suitable for design of fast, low-power circuits, using a reduced number of transistors (as compared to TG and CMOS). Here present new low power GDI technique and small silicon area of VLSI digital circuit as an alternative to complementary metal oxide semiconductor (CMOS) logic design.

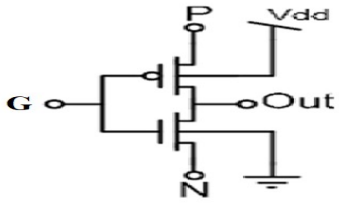

Fig. 4. Modified GDI cell

Table 1:Different logic functions realization using GDI cell

N	P	G	OUT	Function
0	B	A	$A^{I}B$	F1
B	1	A	$A^{I}+B$	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	$A^{I}B+AC$	MUX
0	1	A	A^{I}	NOT
B^{I}	B	A	$A^{I}B+AB^{I}$	XOR
B	B^{I}	A	$A^{I}B^{I}+AB$	XNOR

This logic style suffered from some limitation such as non-full swing output voltage due to threshold drop which means that output either high or low deviate from VDD or GND by the threshold voltage for PMOS or NMOS. Modified GDI technique whereas the cell resembles the primitive cell of GDI. Modified GDI differs from primitive GDI by important difference, bulk terminals of PMOS and NMOS connected with VDD and GND, respectively. This logic style is suitable for fabrication in a standard CMOS process, as well realize improvement in output voltage, power and power delay product compared to basic GDI logic. Although the threshold drop problem, not fully resolved, and the output voltage still degrades.

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B. Block Diagram of Proposed Method

The tool used for simulation purpose is Tanner EDA tool version 13.0. S-Edit increases your design productivity while handling the most complex IC designs. This powerful environment supports fast, 64-bit rendering and cross-probing between schematic, layout, simulator and LVS reporting at net and device levels. Instances in the schematic are linked to simulation models for the designers choice of behavioural modelling from transistor level SPICE to HDL blocks (Verilog or VHDL). Out of the box, S-Edit is integrated with several analog transistor level simulators and mixed signal simulation platforms to suit the users needs. Tanner T-Spice simulation provides fast, accurate simulation for analog and analog/ mixed-signal (AMS) IC designs. T-Spice not only simulates circuits quickly and with a high degree of accuracy, but also is compatible with industry leading standards and integrates easily with the Tanner S-Edit schematic capture tool and Tanner Waveform Viewer. T-Spice includes improved accuracy with advanced modeling, multi-threading support, device state plotting, real-time waveform viewing and analysis, and a command wizard for simple SPICE syntax creation. T-Spice provides extensive support of behavioral models using Verilog-A, expression controlled sources and table-mode simulation. Behavioral models give you the flexibility to create customized models of virtually any device. T-Spice also supports the latest industry models, including BSIM4 and the Penn State Philips (PSP) model and T-Spice supports foundry extensions, including H-SPICE foundry extensions to models. Waveform Editor(W-Edit) displays T-Spice simulation output waveforms as they are being generated during simulation.

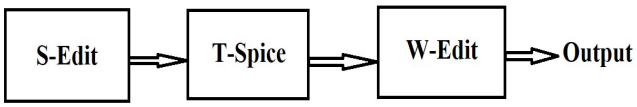

Fig. 5.Block Diagram of Vedic Multiplier using GDI logic

III IMPLEMENTATION

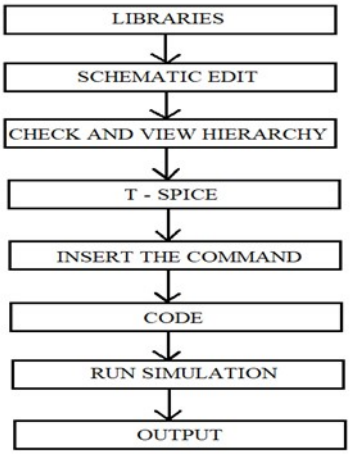

Fig. 6.Flow diagram of Vedic Multiplier using GDI logic

Install Tanner EDA tool. Tanner EDA provides a complete line of software solutions for the design, layout and verification of analog and mixed-signal (A/MS) integrated circuits (ICs). Tanner's solution consist of tools for schematic entry, circuit simulation, waveform probing, full-custom layout editing, placement and routing, netlist extraction, LVS and DRC verification. The boast over 30,000 users of their software. Tanner Designer is an analog verification management tool that tracks all simulations for a project. The tool displays simulation results in a convenient dashboard allowing the team to quickly see which blocks pass or fail specifications and to monitor verification progress. The tool is fully integrated with S-Edit, Analog Fast Spice (AFS), T-Spice, Eldo, and the Tanner Waveform Viewer. Initialize the libraries. Draw the schematic of vedic multiplier in the Schematic – Edit. The libraries should be imported before launching the S-Edit. Then to launch S-Edit, double-click on the S-Edit icon. Tanner S-Edit is an easy-to-use design environment for schematic capture and design entry. It gives you the power you need to handle your most complex mixed-signal IC design capture. S-Edit is tightly integrated with Tanner T-Spice, Analog Fast Spioce (AFS), or Eldo simulators, the Tanner L-Edit IC

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layout tool, and the Calibre LVS and PEX tools. S-Edit helps you meet the demands of today's fast-paced market by optimizing your productivity and speeding your concepts to silicon. A faster design cycle gives you more flexibility in moving to an optimal solution, freeing up more time and resources for process corner validation. Check and view hierarchy, if no errors move to T – Spice.

Tanner T-Spice simulation provides fast, accurate simulation for analog and analog/ mixed-signal (AMS) IC designs. T-Spice not only simulates circuits quickly and with a high degree of accuracy, but also is compatible with industry leading standards and integrates easily with the Tanner S-Edit schematic capture tool and Tanner Waveform Viewer. T-Spice includes improved accuracy with advanced modelling, multi-threading support, device state plotting, real-time waveform viewing and analysis, and a command wizard for simple SPICE syntax creation. Insert the path. Type the code. Run the simulation. Output is viewed in the form of waveforms and numerical values interms of area, power and delay.

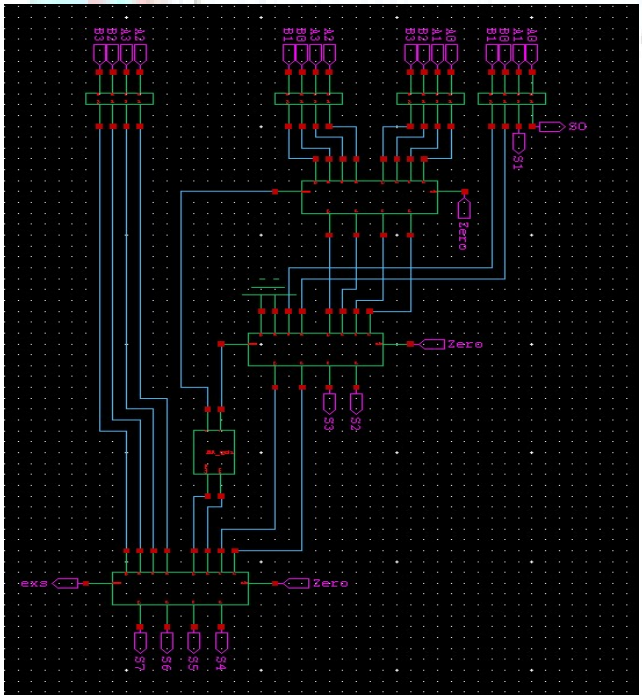

Fig. 7. Schematic of Vedic Multiplier using GDI logic

IV RESULTS AND ANALYSIS

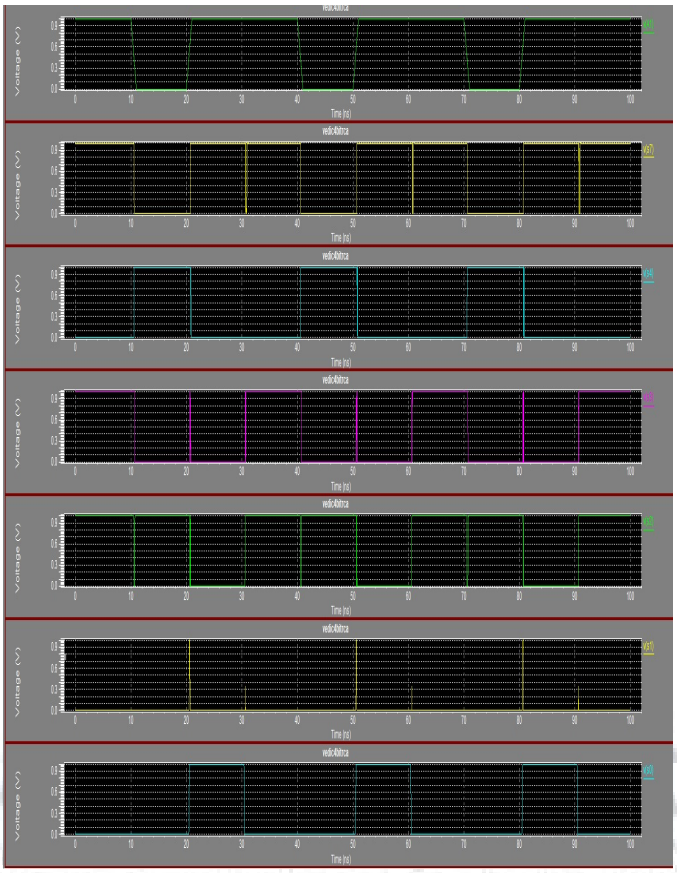

Fig. 8. Output Waveform of RCA using CMOS logic

```
Device and node counts:
          MOSFETs - 828


Power Results
v10 from time 0 to 1e-007
Average power consumed -> 3.564395e-005 watts


MEASUREMENT RESULTS

delay = 4.5857e-010
   Trigger = 1.0100e-008
   Target  = 1.0559e-008
```

Fig. 9. Output of RCA in terms of area, delay and power using CMOS logic

Ripple Carry Adder (CMOS logic)

Ripple Carry Adder using CMOS logic is implemented and output is viewed interms of waveform and numerical value. Fig. 8 shows the

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transient analysis of Ripple Carry Adder using CMOS logic interms of voltage (V) and time (ns), the voltage and time varies from 0 to 10. Fig. 9 shows the numerical values interms of area – 828 nm, power – 0.0356 X 10^{-3} W, delay – 0.4585 X 10^{-9} sec.

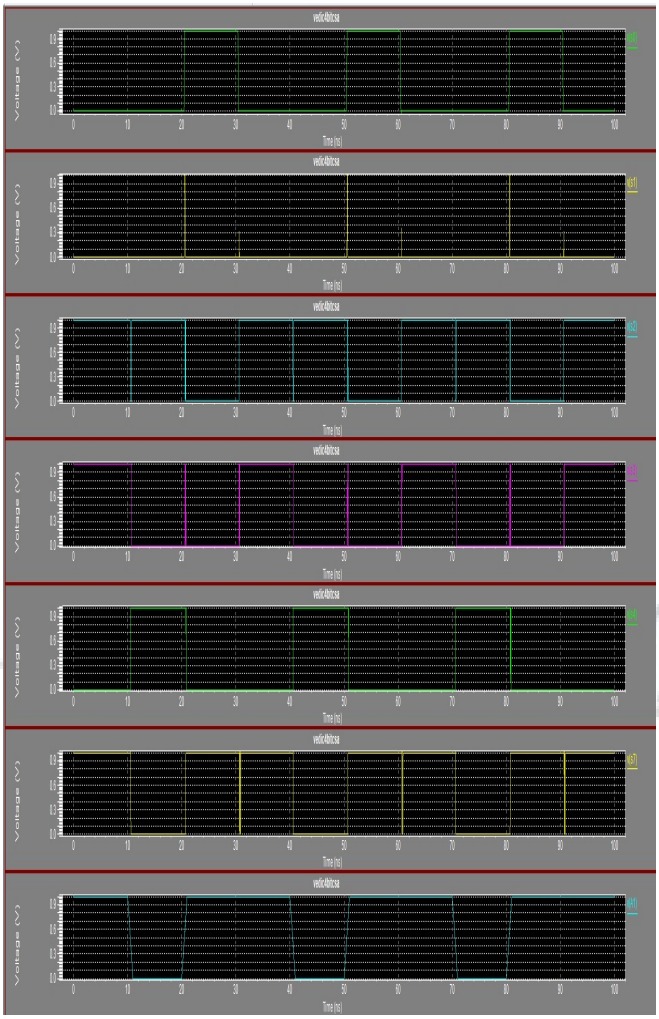

Fig. 10. Output Waveform of CLA using CMOS logic

```
Device and node counts:
            MOSFETs - 1032


Power Results
vl0 from time 0 to 1e-007
Average power consumed -> 1.056534e-003 watts


delay = 5.6317e-010
   Trigger = 1.0990e-008
   Target  = 1.1553e-008
```

Fig. 11. Output of CLA in terms of area, delay and power using CMOS logic

Carry Look – ahead Adder (CMOS logic)

Carry Look – ahead Adder using CMOS logic is implemented and output is viewed interms of waveform and numerical value. Fig. 10 shows the transient analysis of Carry Look – ahead Adder using CMOS logic interms of voltage (V) and time (ns), the voltage and time varies from 0 to 10. Fig. 11 shows the numerical values interms of area – 1032 nm, power – 1.0563 X 10^{-3} W, delay – 0.5631 X 10^{-9} sec.

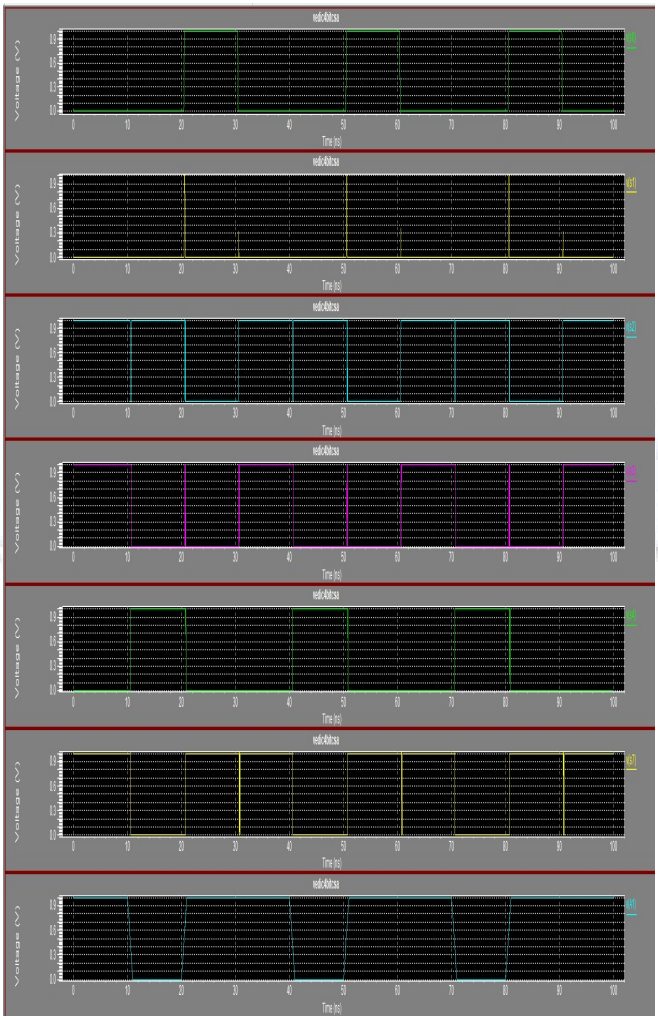

Fig. 12. Output Waveform of CSA using CMOS logic

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```
Device and node counts:
          MOSFETs - 900

Power Results
v10 from time 0 to 1e-007
Average power consumed -> 3.732282e-005 watts

delay = 4.6072e-010
   Trigger = 1.0100e-008
   Target  = 1.0561e-008
```

Fig. 13. Output of CSA in terms of area, delay and power using CMOS logic

Carry Skip Adder (CMOS logic)

Carry Skip Adder using CMOS logic is implemented and output is viewed interms of waveform and numerical value. Fig. 12 shows the transient analysis of Carry Skip Adder using CMOS logic interms of voltage (V) and time (ns), the voltage and time varies from 0 to 10. Fig. 13 shows the numerical values interms of area – 900 nm, power – 0.0373 X 10^{-3} W, delay – 0.4607 X 10^{-9} sec.

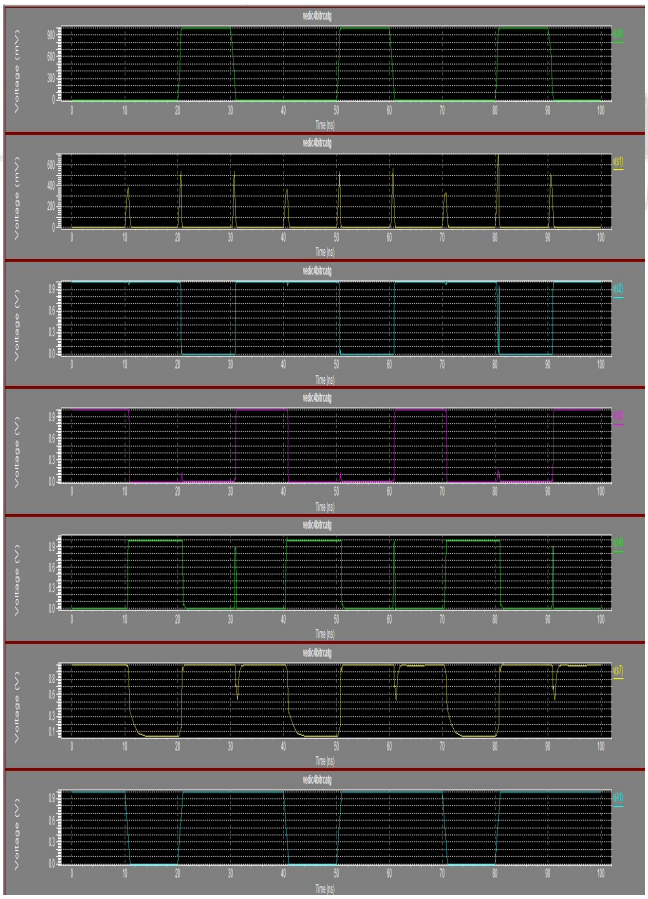

Fig. 14. Output Waveform of RCA using TG logic

```
Device and node counts:
          MOSFETs - 444

Power Results
v10 from time 0 to 1e-007
Average power consumed -> 2.653669e-005 watts

delay = 4.1751e-010
   Trigger = 1.0100e-008
   Target  = 1.0518e-008
```

Fig. 15. Output of RCA in terms of area, delay and power using TG logic

Ripple Carry Adder (TG logic)

Ripple Carry Adder using TG logic is implemented and output is viewed interms of waveform and numerical value. Fig. 14 shows the transient analysis of Ripple Carry Adder using CMOS logic interms of voltage (V) and time (ns), the voltage and time varies from 0 to 10. Fig. 15 shows the numerical values interms of area – 444 nm, power – 0.0265 X 10^{-3} W, delay – 0.4175 X 10^{-9} sec.

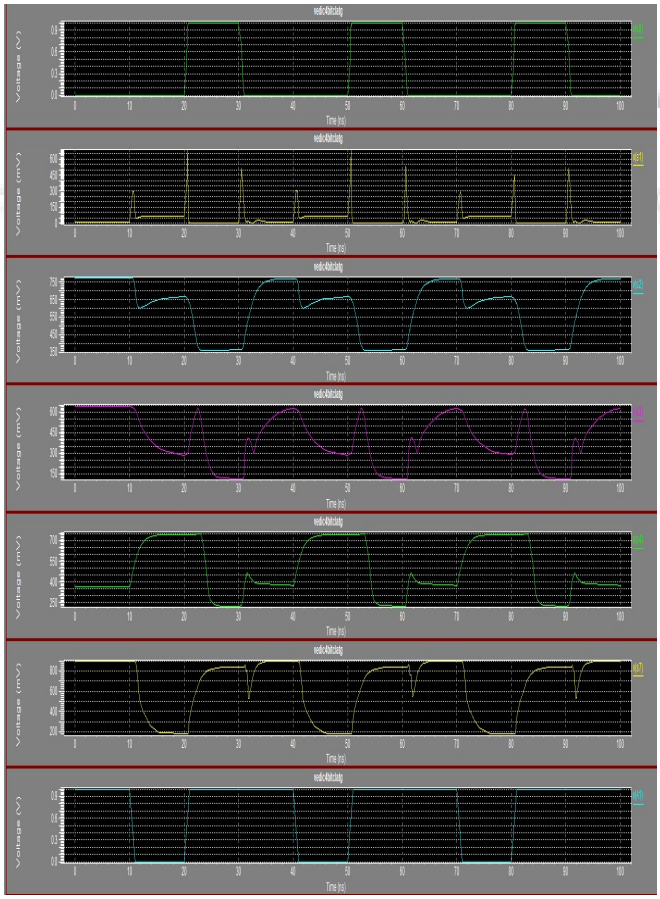

Fig. 16. Output Waveform of CLA using TG logic

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```
Device and node counts:
          MOSFETs - 1104


Power Results
vl0 from time 0 to 1e-007
Average power consumed -> 8.702566e-004 watts


delay = 3.7693e-011
   Trigger = 1.0200e-008
   Target  = 1.0238e-008
```

Fig. 17. Output of CLA in terms of area, delay and power using TG logic

```
Device and node counts:
          MOSFETs - 516


Power Results
vl0 from time 0 to 1e-007
Average power consumed -> 2.962114e-005 watts


MEASUREMENT RESULTS

delay = 4.6290e-010
   Trigger = 1.0100e-008
   Target  = 1.0563e-008
```

Fig. 19. Output of CSA in terms of area, delay and power using TG logic

Carry Look – ahead Adder (TG logic)

Carry Look – ahead Adder using TG logic is implemented and output is viewed interms of waveform and numerical value. Fig. 16 shows the transient analysis of Carry Look – ahead Adder using CMOS logic interms of voltage (mV) and time (ns), the voltage and time varies from 0 to 10. Fig. 17 shows the numerical values interms of area – 1104 nm, power – 0.8702 X 10^{-3} W, delay – 0.0376 X 10^{-9} sec.

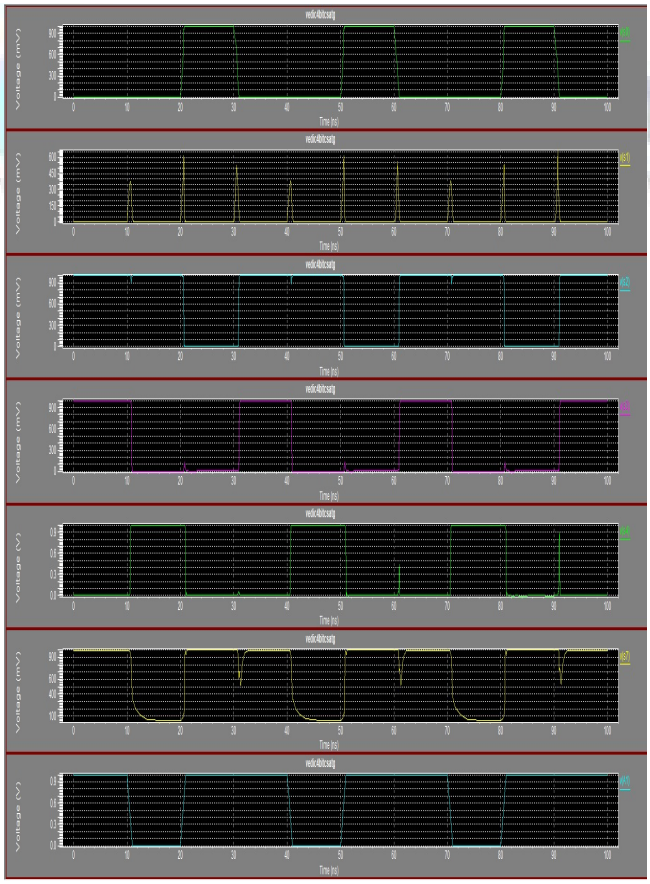

Fig. 18. Output Waveform of CSA using TG logic

Carry Skip Adder (TG logic)

Carry Skip Adder using TG logic is implemented and output is viewed interms of waveform and numerical value. Fig. 18 shows the transient analysis of Carry Skip Adder using CMOS logic interms of voltage (mV) and time (ns), the voltage and time varies from 0 to 10. Fig. 19 shows the numerical values interms of area – 516 nm, power – 0.0296 X 10^{-3} W, delay – 0.4629 X 10^{-9} sec.

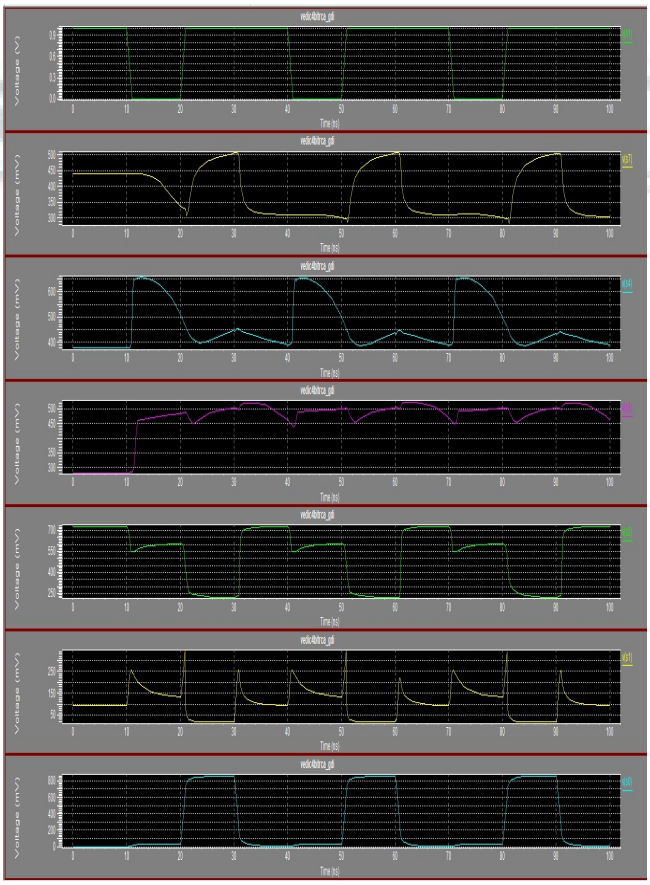

Fig. 20. Output Waveform of RCA using GDI logic

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```
Device and node counts:
          MOSFETs - 206


Power Results
vl0 from time 0 to 1e-007
Average power consumed -> 4.461289e-004 watts


Measurement result summary
   delay =   3.7547e-010
```

Fig. 21. Output of RCA in terms of area, delay and power using GDI logic

Ripple Carry Adder (GDI logic)

Ripple Carry Adder using GDI logic is implemented and output is viewed interms of waveform and numerical value. Fig. 20 shows the transient analysis of Ripple Carry Adder using CMOS logic interms of voltage (mV) and time (ns), the voltage and time varies from 0 to 10. Fig. 21 shows the numerical values interms of area – 206 nm, power – 0.4461 X 10^{-3} W, delay – 0.3754 X 10^{-9} sec.

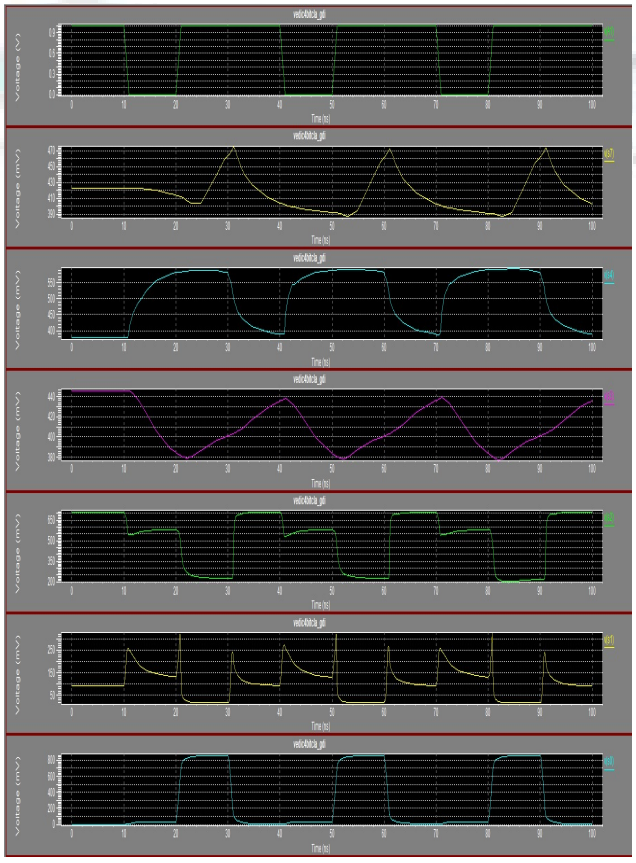

Fig. 22. Output Waveform of CLA using GDI logic

```
Device and node counts:
          MOSFETs - 386


Power Results
vl0 from time 0 to 1e-007
Average power consumed -> 7.793233e-004 watts
Max power 1.277644e-003 at time 3.09894e-008


Measurement result summary
   delay =   1.4872e-011
```

Fig. 23. Output of CLA in terms of area, delay and power using GDI logic

Carry Look – ahead Adder (GDI logic)

Carry Look – ahead Adder using GDI logic is implemented and output is viewed interms of waveform and numerical value. Fig. 22 shows the transient analysis of Carry Look – ahead Adder using CMOS logic interms of voltage (mV) and time (ns), the voltage and time varies from 0 to 10. Fig. 23 shows the numerical values interms of area – 386 nm, power – 0.7793 X 10^{-3} W, delay – 0.0148 X 10^{-9} sec.

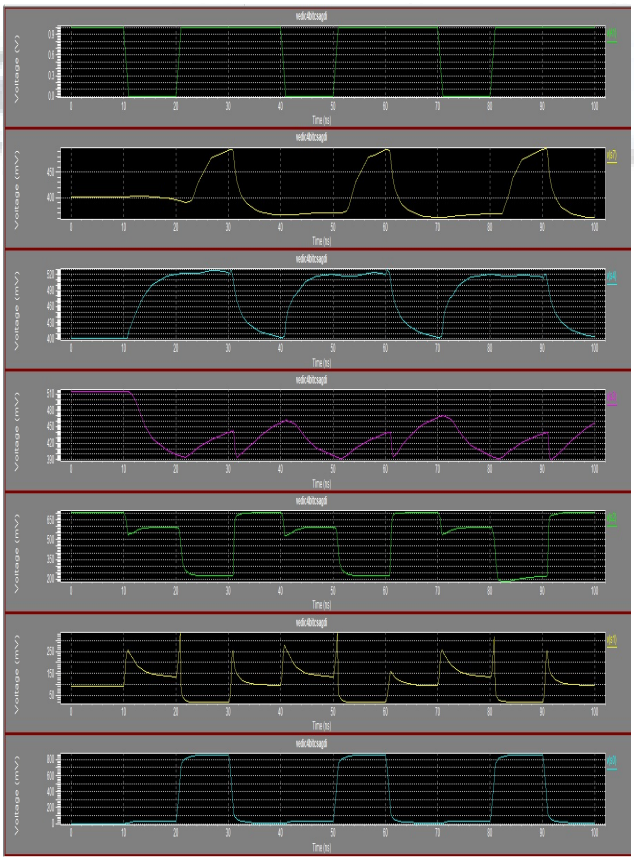

Fig. 24. Output Waveform of CSA using GDI logic

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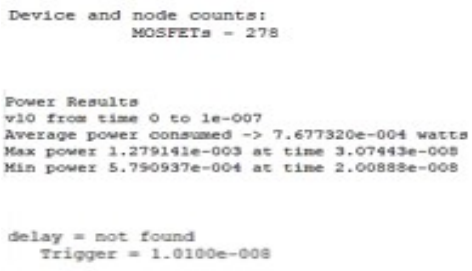

Fig. 25. Output of CSA in terms of area, delay and power using GDI logic

Carry Skip Adder (GDI logic)

Carry Skip Adder using GDI logic is implemented and output is viewed interms of waveform and numerical value. Fig. 24 shows the transient analysis of Carry Skip Adder using CMOS logic interms of voltage (mV) and time (ns), the voltage and time varies from 0 to 10. Fig. 25 shows the numerical values interms of area – 278 nm, power – 0.7677 X 10^{-3} W, delay – 0 sec.

Comparison Table

CMOS Logic

VEDIC MULTIPLIER	AREA in (nm)	POWER in (W)	DELAY in (sec)
RCA	828	0.0356 X 10^{-3}	0.4585 X 10^{-9}
CLA	1032	1.0563 X 10^{-3}	0.5631 X 10^{-9}
CSA	900	0.0373 X 10^{-3}	0.4607 X 10^{-9}

TG Logic

VEDIC MULTIPLIER	AREA in (nm)	POWER in (W)	DELAY in (sec)
RCA	444	0.0265 X 10^{-3}	0.4175 X 10^{-9}
CLA	1104	0.8702 X 10^{-3}	0.0376 X 10^{-9}
CSA	516	0.0296 X 10^{-3}	0.4629 X 10^{-9}

GDI Logic

VEDIC MULTIPLIER	AREA in (nm)	POWER in (W)	DELAY in (sec)
RCA	206	0.4461 X 10^{-3}	0.3754 X 10^{-9}
CLA	386	0.7793 X 10^{-3}	0.0148 X 10^{-9}
CSA	278	0.7677 X 10^{-3}	0

V CONCLUSION

Gate Diffusion Input is the VLSI technique to reduce the dynamic and static power dissipation in digital circuits. By using this technique various digital circuits can be designed with low transistor count as compare to CMOS designs which results in low power dissipation. GDI technique is power efficient technique for designing digital circuit that consumes less power as compare to most commonly used CMOS technique. GDI also has an advantage of minimum propagation delay, minimum area required and area 0f digital logic circuits.

A. Conclusion

In this project 4-bit vedic multiplier using RCA adder, CLA adder and CSA adder using GDI technique has been compared with TG and CMOS technology to find out which occupies less area and delay. All the designs are simulated using Tanner EDA software with 32nm technology file. Simulation results show that that the proposed GDI based vedic multiplier offers less area and delay compared to both CMOS as well as TG based vedic multiplier designs. From the results it is observed that the area and delay is reduced area - 18% and delay - 34.92%.

B. Future Scope

One of the most important hardware blocks in processors is the multiplier circuit module. Area, power, and delay rule as primary factors deciding VLSI design methodologies. The ancient system of Indian mathematics being the Vedic mathematics, rediscovered from the Vedas, is more simplified, faster and accurate as compared to normal multiplication methods. The primary advantage of gate-diffusion input (GDI) logic is helping in reduced transistor count. Hence, the combination of these approaches of Vedic multiplication implemented using GDI logic results in reduced propagation delay time, lower power consumption, and less silicon area. Multipliers are used in the building blocks of several processors. Conventional multiplication is time consuming and lengthy process, to overcome this the circuit designers must develop speedy multipliers.

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Vedic multipliers can be utilized for high speed multiplication process. In designing of CMOS circuits an issue of area is always there, to reduce this Gate Diffusion Input (GDI) technique can be used.The GDI concept assit in reduction of Transistor Count (TC).

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