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Design and Implementation of Phase-Locked Loop using CMOS Technology

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Abstract: The Phase-Locked Loops (PLLs) are fundamental components in contemporary electronic systems, with applications ranging from clock generation and frequency synthesis to data recovery. A PLL is a closed- loop control system that synchronizes its output signal's phase and frequency with a reference input signal. This synchronization is vital for the functionality of various electronic devices, such as communication systems, microprocessors, and data storage solutions. To address the growing need for high-performance PLLs, the integration of VLSI and CMOS technologies has become essential. Key design considerations include power consumption, noise, and phase noise performance. This project highlights the use of Tanner EDA tools and underscores the importance of a systematic, iterative approach in PLL design to achieve optimal results.

Keywords: Phase-Locked Loop (PLL), Very Large Scale Integration (VLSI), Complementary Metal-Oxide-Semiconductor (CMOS), Tanner EDA Tool.

I. INTRODUCTION

In the ever-evolving landscape of modern electronics andsemiconductor technology, the demand for precise and adaptable clock generation solutions is paramount[7]. Phase-Locked Loops (PLLs) stand at the forefront of this endeavor, serving as vital components in a multitude of applications, from wireless communication systems and microprocessors to data converters and more[4]. The ability to generate stableand precise output frequencies, coupled with low power consumption and reduced noise, has made PLLs indispensable in the digital age.

The project at hand is a significant response to this demand, aiming to design and implement a PLL using Complementary Metal-Oxide-Semiconductor (CMOS) technology[7]. The challenges it seeks to address are multifaceted, encompassing the need for versatile frequency synthesis, low power consumption, and noise reduction. Furthermore, the project recognizes the inherent variability in CMOS manufacturing processes and endeavors to ensure compatibility with the most modern fabrication techniques, down to nanometre-scale transistor technologies. The efficient utilization of silicon real estate is another critical aspect that promises to reduce manufacturing costs and facilitate integration into compact semiconductor devices.

In the heart of our increasingly interconnected world, where data is transmitted, processed, and managed at unprecedented rates, the role of PLLs becomes even more pivotal[4]. These dynamic circuits are tasked with maintaining precise synchronization and generating clock signals, ensuring that complex digital systems operate seamlessly. However, the ever accelerating pace of technological advancement necessitates novel solutions that not only deliver on the promise of precision but also cater to the ever-increasing demand for energy efficient and compact devices[6].

The focus of this project is to rise to the challenge by harnessing the capabilities of CMOS technology, a foundational pillar of modern semiconductor manufacturing[7]. The scope encompasses the creation of a PLL architecture capable of producing stable and accurate output frequencies, spanning a broad spectrum ofprogrammable options[4]. By addressing

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the perennial issue of power consumption, the project aims to pave the way for PLLs that are not only high performing but also eco- friendly, making them suitable for portable and battery- operated applications.

The fundamental components of a PLL include a Phase Detector, Frequency Divider, Voltage Controlled Oscillator (VCO), and Loop Filter. PLLs generate signals with a phase that aligns with a given input signal. They are used to produce signals at multiples of the original frequency or at programmable frequencies, making them effective for tracking and locking to the phase and frequency variations ofinput signals. When the phase and frequency of the input signals match, the PLL is considered to be locked, meaning the phase difference between the reference signal and the input signal is a known value. Due to their versatility, PLLs are extensively used in high-performance microprocessors and modern communication systems. Additionally, they are employed in various applications, such as motor speed control, frequency modulation and demodulation, clock recovery, generating carrier signals from suppressed input signals, and synchronizing local clocks with other desired signals.

II. PROPOSED SYSTEM

The main goal of this work is to design and develop the essential components of a PLL, including the phase detector (PFD), voltage controlled oscillator (VCO), loop filter, and frequency divider, with a focus on minimizing power consumption. The performance in terms of power efficiency and frequency selection in the frequency divider is primarily influenced by the VCO and the frequency divider itself. A key aspect of the proposed PLL design is that the VCO will be controlled via a switch control mechanism, eliminating the need for an external control voltage. The power consumption and frequency selection capabilities of the frequency divider are constrained by the VCO and the frequency divider. Figure 1 illustrates the block diagram of abasic PLL, which consists of (i) a Phase Detector (PFD), (ii)a Low Pass Filter (LPF), and (iii) a Voltage Controlled Oscillator (VCO). In frequency generation applications, a frequency divider, implemented with an 'N' bit synchronous counter, is placed between the VCO and the PFD. In this setup, the VCO generates a frequency that is 'N' times the original frequency when the counter is used.

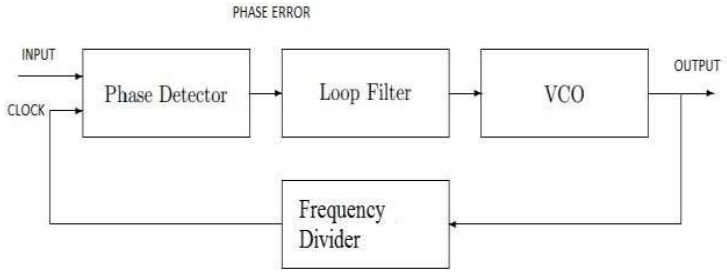

Fig 1 : Block diagram of the PLL

A. Phase-Frequency Detector

A Phase-Frequency Detector, commonly abbreviated as PFD, is a crucial component in many electronic systems, including Phase-Locked Loops (PLLs), where it plays a fundamental role in maintaining synchronization and precise control of phase relationships between signals. The primary function of a phase detector is to compare the phase of two input signals and generate an output signal that indicates their phase difference. Phase Comparison: A phase detector essentially acts as a phase comparator. It takes two input signals: a reference signal (often referred to as the "reference" or "input") and a feedback signal (the "feedback" or "output"). It continuously assesses the phase difference between these signals. Below figure 2 represents the schematics of the Phase-Frequency detector.

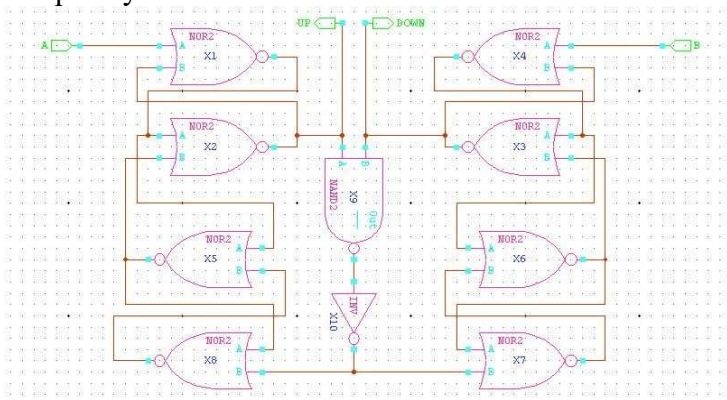

Fig 2 : Phase-Frequency Detector Schematics

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B. Charge Pump circuit and Loop Filter

In a PLL design, the Charge Pump is implemented using integrated circuit technology and includes pull-up and pull- down transistors along with an on-chip capacitor. The Phase Frequency Detector (PFD) generates UP and DOWN signalsthat act as switches; when the UP signal is active, the DOWN signal is inactive, and vice versa. This ensures that only one signal is active at any given time, facilitating proper operation of the Charge Pump.Charge pump can be easily implemented using MOSFETs as shown on the Figure 3. Here M1 and M2 operates as current sources, and M3 and M4 operate as switches. An immediate drawback of this implementation can be seen as the inputs to the charge pump are reaching CP at different times, due to the delay caused by the inverter. This error can suppressed by inserting a transmission gate between Qb and the gate of M3, equalizing the delays. Loop filters are used to shape the frequency response and dynamics of control loops. In systems like PLLs, they are responsible for controlling the bandwidth and damping factor of the loop. Below figure 4 shows schematics of Loop filter.

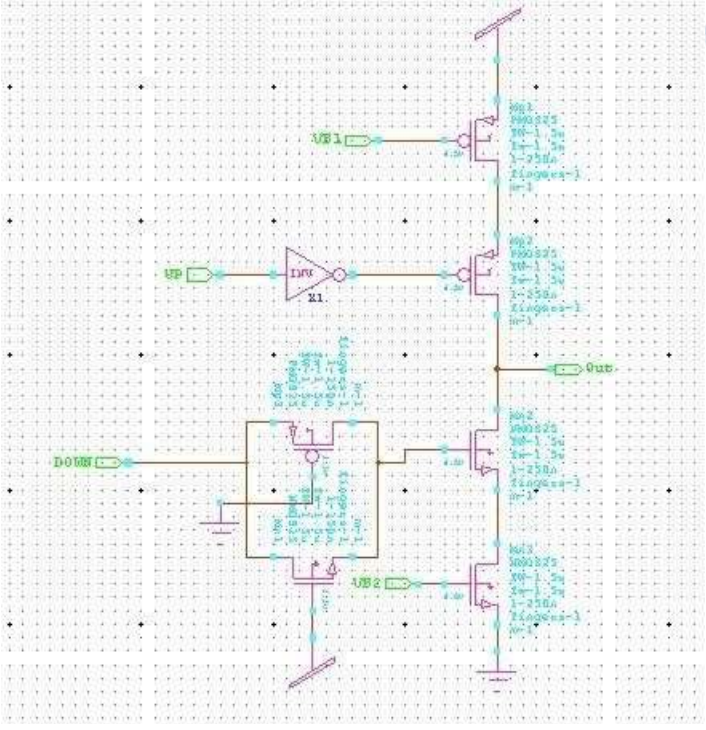

Fig 3 : Schematics of Charge Pump Circuit

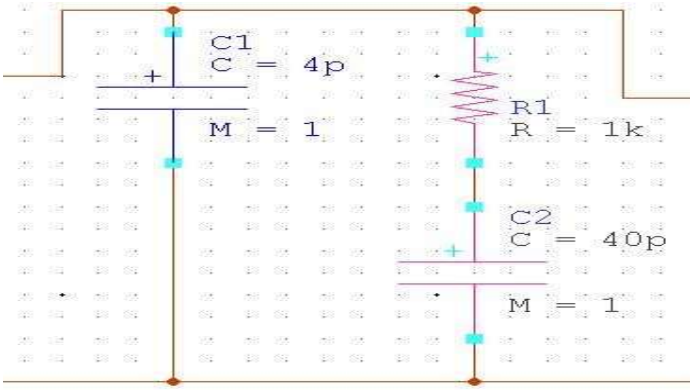

Fig 4 : Schematics of Loop filter

C. Ring Oscillator and VCO

An oscillator produces periodic output, generally in the form of voltage. Most ap plications require to control the output frequency of the oscillator. Here is where VCO comes into picture. VCO provides us the capability to control the frequency of the oscillator by tuning its input voltage i.e VCO is a voltage to frequency converter. There are several architectures for designing VCO. Here we choose to design and analyze Current Starved VCO. Current Starved architecture is preferred as it is less sensitive to the voltage variation in VDD. The basic structure of VCO is designed using Ring Oscillator and further to implement the current starved architecture current mirrors are used. Below is schematics of Ring oscillator Figure 5 and VCO Figure 6.

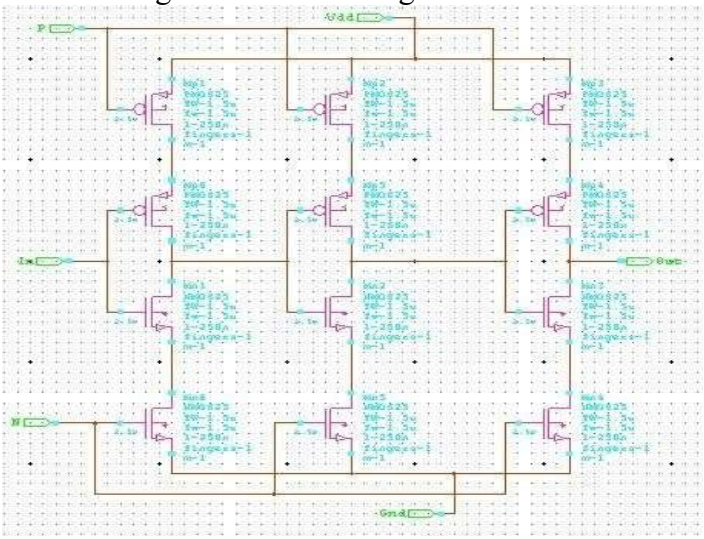

Fig 5 : Ring oscillator

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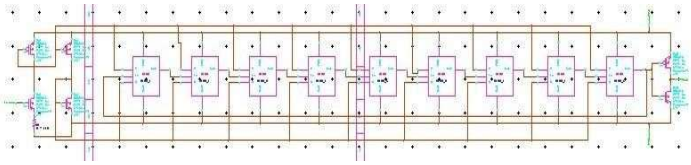

Fig 6 : VCO schematics

D. Frequency Divider

Divide-by-2 frequency divider is used to provide feedback form CSVCO to PFD. It is simply implemented using D flip flops, as shown in the Figure 7. This structure reduces the time jitter of the VCO.

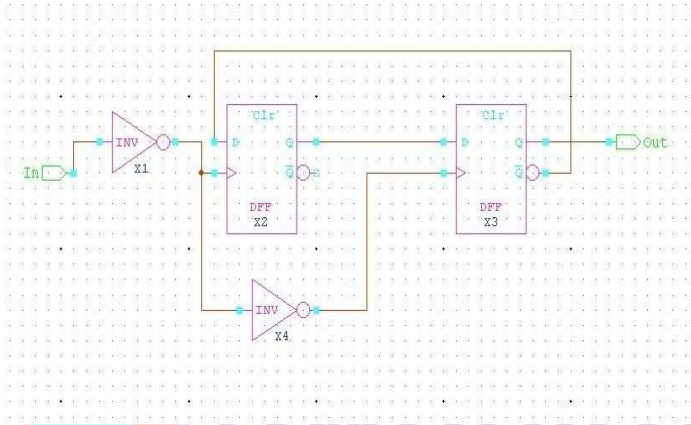

Fig 7 : Frequency divider schematics

Below is the final test circuit for PLL, which is implemented by combining all the components. First is without Frequency Divider and second is with Frequency Divider.

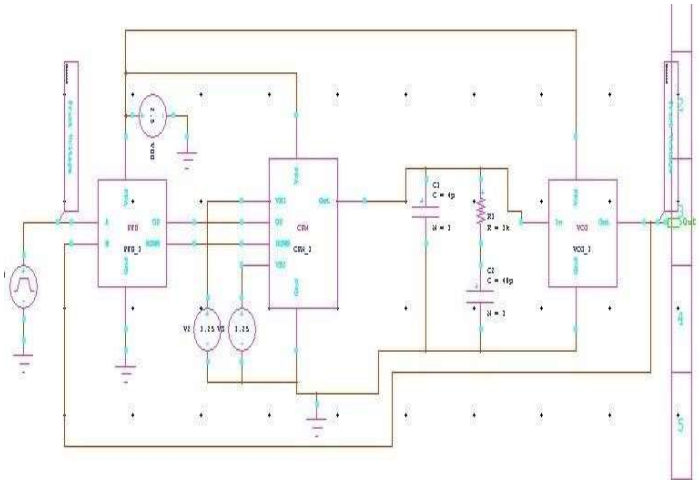

Fig 8 : PLL without frequency divider

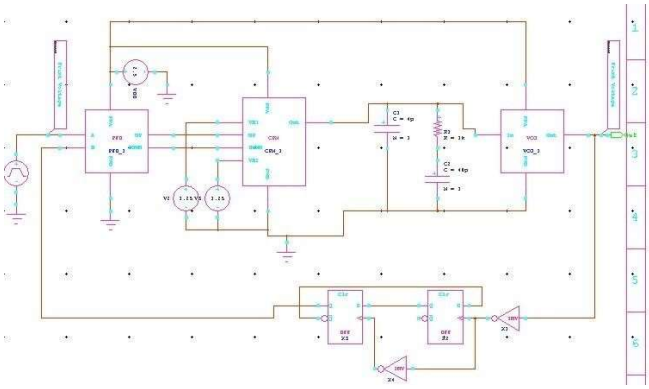

Fig 9 : PLL with frequency divider

The table below shows the parameters and values for theproposed system design.

PARAMETERS	Values
CMOS technology	250nm
Supply voltage	2.5V
VCO centre frequency	48MHz
Low pass filter	R = 1kΩ C1 = 4pF C2 = 40pF
Input signal	V1 = 0V V2 = 2.5V Delay = 10ns Rise = 100ps Fall = 100ps Period = 20ns PW = 10ns
Distance of tapered slot from the central point (D)	8.5
Mouth opening of two tapered slots (M2)	9.4

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III RESULTS AND DISCUSSION

The simulations of each part of PLL is obtained and studied.

A. Phase Frequency Detector Simulation

Figure 10 shows the output of a phase frequency detector in which its output UP goes high whenever Vref is leading Vfb and DOWN goes high when ever Vref lagging behind Vfb.

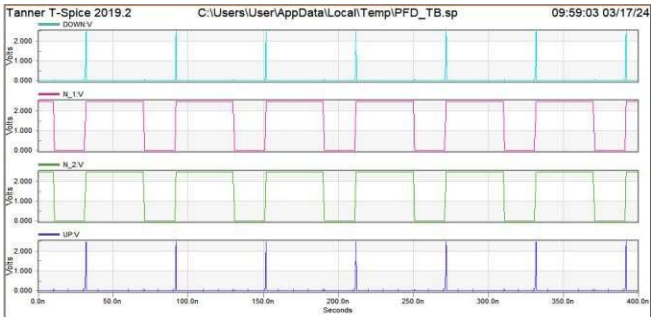

Fig 10 : PFD Simulation

B. VCO Simulation

Figure 11 shows simulation of VCO. For control voltage 2.5V it generates a pulse signal of frequency 90MHz.

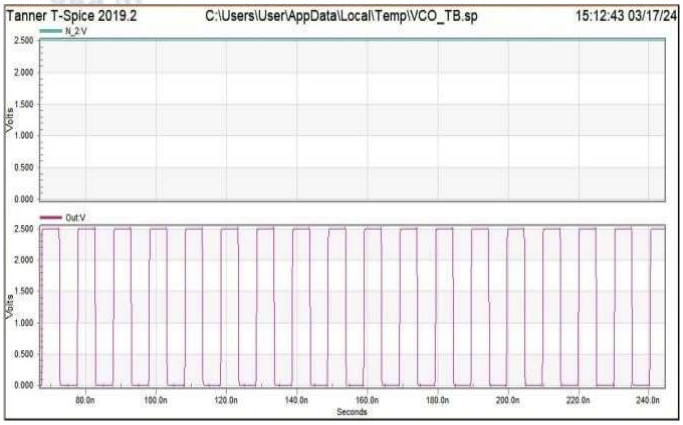

Fig 11 : Simulation of VCO

C. Frequency Divider Simulation

Fig 12 shows the result of a frequency divider. The input signal frequency is divided by a factor of 2.

Fig 12 : Frequency Divider Simulation studied.

D. Phase-Locked Loop Simulation

Figure 13 presents the simulation output of a digital phase-locked loop (DPLL) operating with a voltage-dependent free-running frequency. The input and output voltage-controlled oscillations are in phase, illustrating the phase alignment between them. Figure 14 displays the simulation output of a PLL that incorporates a frequency divider.

Fig 13 : PLL Simulation without frequency divider

Fig 14 : PLL Simulation with frequency divider

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E. Performances Analysis

Parameters	Value
Lock time	190ns
Settling time	30ns
Jitter	1ns
Power Consumption Without frequency divider	0.894mW
Power Consumption withfrequency divider	0.704mW

IV CONCLUSION

In conclusion, this project work on Phase-Locked Loops (PLLs) has provided a comprehensive exploration of key components within PLL systems, specifically focusing on the Voltage-Controlled Oscillator (VCO), Phase Frequency Detector (PFD), and loop filter. The simulation of individual components, including the phase detector, loop filter, voltage-controlled oscillator (VCO), and frequency divider, provided valuable understanding of their respective roles and characteristics within the overall PLL architecture. Lock time is 190ns, settling time is 30ns and jitter 1ns and power consumed is around 0.704mW.

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