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Design of Low Dropout Regulator for Wearable Healthcare System Device using 45nm CMOS Technology

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Abstract: The project proposes a stable, high Power Supply Rejection Ratio (PSRR), and minimal Low Dropout Regulator (LDO) circuit architecture for wearable devices. The design uses a conventional PMOS pass transistor due to its low quiescent current, minimal circuit complexity, and small area requirements. An RC Miller compensation circuit is incorporated to improve stability. The proposed LDO was designed and simulated using CMOS 45nm process technology in the Cadence analog design environment. Simulation results show that the LDO regulates a 1.6V output from a 1.8V supply with a minimum dropout voltage of 200mV, using a 1V reference voltage. The design is to enhance the performance of 38dB, a phase margin of 68.57°, a PSRR of 50.85dB at 1kHz, Improving Power Efficiency by using Adaptive Biasing which reduce power consumption by dynamically adjusting the bias current based on load conditions and Increasing Error Amplifier at a higher-gain amplifier can improve PSRR at higher frequencies.

Keywords: Low dropout regulator, PSRR (Power supply rejection ratio), RC miller, Stability, Phase margin, PMOS pass Transistors.

I. INTRODUCTION

The design of a Low Dropout Regulator (LDO) for wearable healthcare system devices using 45nm CMOS technology focuses on delivering a stable and efficient power supply essential for the reliable operation of biomedical sensors and low-power integrated circuits.

In these applications, where compactness, low noise, and prolonged battery life are critical, an LDO plays a vital role by regulating voltage with minimal dropout and maintaining consistent performance under varying load conditions. The use of advanced 45nm CMOS technology allows for high integration, reduced power consumption, and improved transistor performance, making it ideal for miniaturized healthcare devices. This design typically incorporates a PMOS pass transistor for efficient low-voltage regulation, a

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high-gain error amplifier to ensure precise voltage control, and RC Miller compensation to enhance stability and transient response.

Wearable healthcare technology has seen tremendous growth due to its ability to provide continuous, real-time monitoring of physiological parameters. These systems are especially valuable in chronic disease management, fitness tracking, and early health diagnostics.

II. SYSTEM DESIGN AND ARCHITECTURE

The proposed LDO consist of PMOS pass transistor, which serves as the primary regulating element. A PMOS transistor is chosen due to its low dropout characteristics and high efficiency, which are crucial for wearable devices operating on limited battery power. The design is implemented using CMOS 45nm technology, which offers advantages such as low power consumption, high integration capability, and improved transistor performance. A well-defined architecture is established, incorporating an error amplifier to regulate the output voltage effectively.

The error amplifier plays a crucial role in maintaining a high gain, ensuring precise control over the pass transistor by comparing the output voltage with a stable reference voltage. A 1V reference voltage is used to provide accurate regulation, preventing fluctuations that could impact the performance of healthcare monitoring sensors. To enhance stability, this compensation technique involves placing a resistor and capacitor in the feedback path of the error amplifier to control the phase margin and prevent oscillations. Stability analysis is conducted using frequency response simulations to ensure that the phase margin remains above the required threshold, typically around 60 degrees, to avoid instability.

III METHODOLOGY

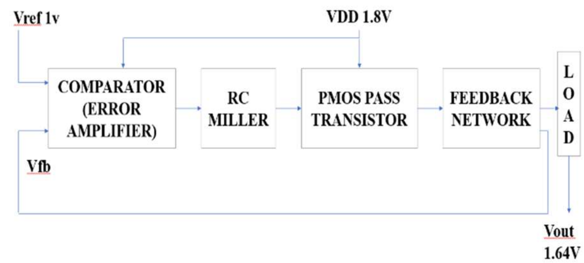

Fig 1 block diagram of Conventional LDO Architecture

The Figure 1 illustrates the block diagram of the Low Dropout (LDO) Regulator illustrates a simplified but efficient architecture designed for wearable healthcare devices. The system begins with a power input (VDD) of 1.8V, which serves as the primary energy source. This voltage is regulated down to 1.64V by the LDO to supply sensitive components in wearable systems. At the core of the LDO is the reference voltage source (Vref), typically set at 1V, which provides a stable benchmark against which the output voltage is compared. The error amplifier, a high-gain differential amplifier, receives both the reference voltage and the feedback voltage (Vfb) from the output. It generates an error signal based on the difference between these two inputs. This signal controls the PMOS pass transistor, which acts as a variable resistor, adjusting its resistance to regulate current flow and maintain a consistent output voltage.

The feedback network, composed of a resistor divider, continuously samples the output voltage and sends a portion back to the error amplifier for comparison, forming a closed-loop system. To ensure stability, especially under varying load conditions, an RC Miller compensation circuit is placed between the output and input of the error amplifier. This configuration effectively manages frequency response and phase margin. Finally, the regulated output voltage is delivered to the load, which represents the actual wearable healthcare device or system. The entire block diagram emphasizes low power consumption, high stability, and noise rejection-features essential for reliable performance in wearable medical applications.

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IV IMPLEMENTATION

The implementation of Low Dropout Regulator (LDO) in CMOS technology, designed to provide a stable and regulated output voltage using a low input-to-output voltage difference (dropout). It operates by comparing a reference voltage to a scaled version of the output voltage through a feedback network. An error amplifier processes this difference and drives a PMOS pass transistor, which controls the amount of current flowing from the supply to the output. The design includes compensation techniques to ensure loop stability and proper transient response, as well as biasing circuits to maintain consistent operating points across process and temperature variations. This type of LDO is commonly used in power management for sensitive analog and digital blocks in SoCs and wearable devices.

RC Miller compensation, are used to control the phase margin and ensure stable operation. By carefully designing the compensation network, the error amplifier can achieve both high gain and sufficient phase margin, preventing undesirable oscillations that could disrupt the voltage regulation process.

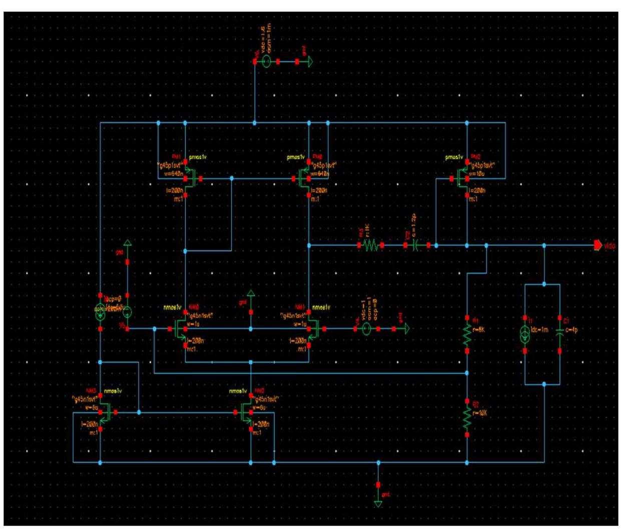

Fig 2: Schematic of LDO (Low DropOut Regulator)

Fig 2 illustrates, The schematic of Low Dropout Regulator (LDO) designed using CMOS analog building blocks in Cadence Virtuoso. The primary function of this circuit is to generate a stable output voltage (Vdo) from a higher supply voltage (Vdd), while maintaining a small dropout voltage and ensuring high stability and regulation under varying load and supply conditions. The design follows a standard architecture involving a two-stage error amplifier, a PMOS pass element, a feedback voltage divider, and a Miller compensation network for frequency stability. The operation is based on negative feedback: the error amplifier compares the reference voltage (Vref) with a portion of the output voltage, and based on the difference, adjusts the gate of the pass transistor to regulate the output.

In the design of an LDO regulator, the error amplifier is typically implemented using a differential pair architecture to provide high gain and linear operation. The differential pair compares the reference voltage with the output feedback voltage and produces an amplified error signal that drives the pass transistor. To enhance performance, additional gain stages may be introduced to further amplify the error signal and improve loop accuracy. However, achieving high gain while maintaining stability is a challenge, as excessive gain can lead to instability and oscillations. This is where compensation techniques.

Transistors Involved is NM0, NM1 (differential pair), PM0, PM1 (PMOS current mirror load), NM0 and NM1 form a differential pair. One gate is connected to the reference voltage (Vref) and the other to the feedback voltage from the output. Their sources are tied together and connected to a tail current source (usually NM3 or NM5), which defines the operating current of the stage, PM0 and PM1 act as a current mirror, providing an active load. The current through NM0 is mirrored into the drain of NM1 via PM0/PM1, the voltage at the output of the mirror (drain of NM1) represents the amplified differential signal. This configuration provides high differential gain and good common-mode rejection, the purpose is to detect any

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difference between Vref and the scaled output and convert it into a control voltage.

Components Used are Capacitor, Series resistor, the capacitor C1 is connected from the output of the second stage (drain of NM_2) back to the output of the first stage (drain of NM_1). This forms a Miller capacitor, which introduces a dominant pole in the amplifier's frequency response. R2, in series with C1, introduces a left-half plane zero, which improves phase margin and stabilizes the loop. This compensation method is key to avoiding oscillations and ensuring good transient performance.

Components Used are R3 and R4, this is a simple resistive voltage divider from Vdo. It taps a fraction of the output voltage and feeds it back to the negative input of the differential amplifier. The divider ratio determines the output voltage using the formula:

$$Vdo = Vref \times (1 + R3\,R4) \qquad \ldots\ldots.\ (1)$$

This negative feedback loop automatically adjusts PM4 to maintain the target output voltage, any deviation in Vdo is sensed by this network and corrected by the control loop.The load is connected at the node labeled Vdo, which is the output of the PMOS pass transistor (PM4). It appears that a resistor labeled Rload is connected between Vdo and ground, representing a resistive load, this resistor models the static power consumption of the circuit that uses the regulated voltage. The load draws output current from the LDO, As the load changes (e.g., more current demand), the output voltage tends to drop, the feedback mechanism senses this drop, and the error amplifier responds by adjusting the gate of PM4 to allow more current, restoring Vldo. The regulator's ability to maintain Vdo under load variation is called load regulation.

V RESULTS

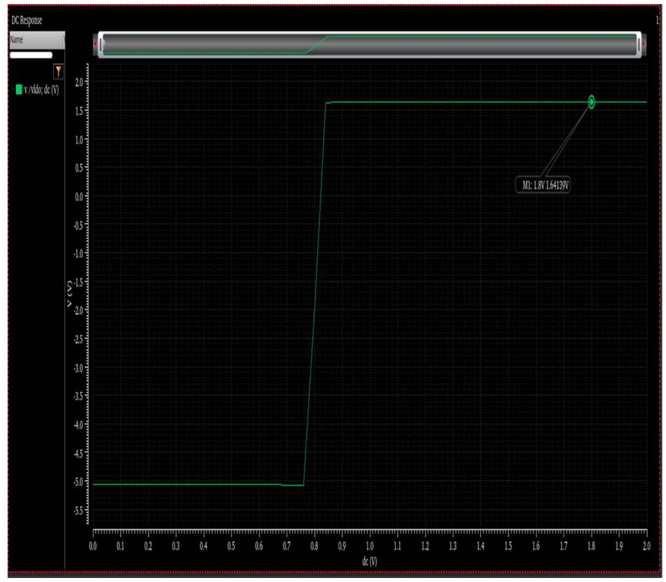

Fig 3 Output Voltage of 1.64409v at input voltage 1.8v

The Fig 3 illustrates, the DC transfer characteristics of the designed Low Dropout (LDO) voltage regulator, where the output voltage is plotted against the varying input voltage. This analysis is crucial to evaluate the line regulation capability of the LDO. As seen in the red curve corresponding to the output voltage (vldo), the regulator initially shows a rapid rise in output as the input voltage increases from 0V. At the point labeled M2, when the input voltage is approximately 163mV, the output has reached around 1.6378 V, indicating that the regulator begins to operate and respond to the input supply. As the input voltage continues to rise, the output voltage stabilizes near the desired target of 1.8V.

This is clearly observed at marker M1, where the input voltage is 1.8 V and the output voltage is 1.6441 V. Beyond this point, the output voltage remains nearly constant despite further increases in the input, which demonstrates effective regulation. The flat segment of the output curve confirms that the LDO maintains a stable output with minimal deviation, highlighting good line regulation performance. This behavior ensures that the LDO can reliably supply a constant voltage to sensitive

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electronic components, such as those in wearable healthcare systems, even when the supply voltage fluctuates within a certain range.

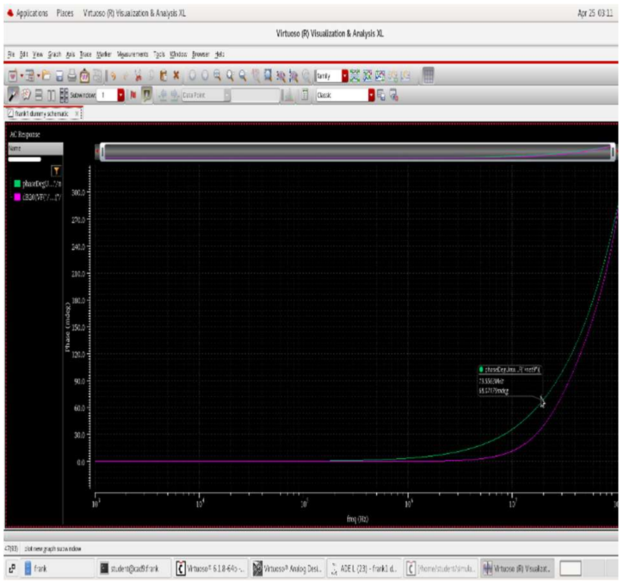

Fig 4 Stability response of proposed LDO with compensation

The Fig 4 illustrates, the AC response plot of the designed LDO regulator illustrates its frequency behaviour in terms of gain and phase across a wide frequency range. The purple curve represents the gain (in dB), while the green curve indicates the phase shift (in degrees). From the simulation, the phase margin is observed to be approximately 68.07° at a frequency of 19.53MHz, with a corresponding gain of about 8.84dB. The values confirm that the LDO regulator exhibits good stability, as a phase margin above 45° typically ensures stable operation without oscillations. The relatively flat gain and smooth phase variation across the frequency spectrum further indicate that the regulator can maintain its performance and resist disturbances across varying dynamic conditions, making it highly suitable for wearable healthcare system applications.

In wearable medical devices, sensors, and portable electronics. Careful design of the error amplifier, compensation techniques (like Miller compensation), and pass element selection ensures stability, fast transient response, and high-power supply rejection ratio (PSRR). Thus, the LDO remains an indispensable solution in the design of robust and reliable power management units.

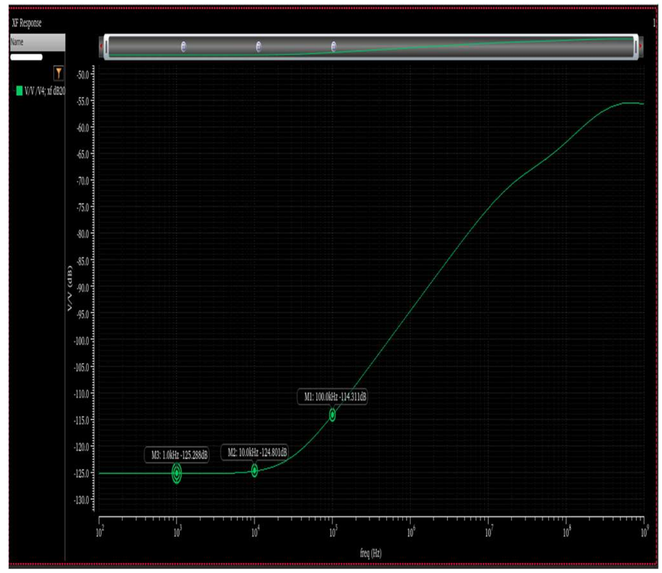

Fig 5 Stability Response of PSRR(Power Supply rejection Ratio)

The Fig 5 represents the graph of the Power Supply Rejection Ratio (PSRR) or Power Supply Ripple Rejection (PSRR) response of the LDO regulator, as simulated using Cadence Virtuoso. It demonstrates how effectively the LDO suppresses variations or ripples in the input supply voltage from propagating to the output. The Y-axis shows the rejection level in decibels (dB), while the X-axis represents frequency in Hz on a logarithmic scale. The green curve depicts the transfer function Vout /Vin V_{out}/V_{in} Vout/Vin in dB, which quantifies how much noise from the input supply is attenuated at the output across a range of frequencies.

From the markers in the plot, it is observed that at lower frequencies such as 1 kHz (M3) and 10kHz (M2)—the PSRR is around -125 dB and -124.89 dB, respectively. At 100 kHz (M1), the rejection slightly degrades to -114.31 dB. This performance indicates excellent PSRR at low frequencies, which is particularly important for wearable healthcare

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systems that require clean and noise-free voltage supplies for sensitive analog front ends and bio-signal acquisition circuits. The decreasing PSRR at higher frequencies is typical for LDOs, but the observed results still demonstrate strong rejection capabilities, confirming that the designed regulator is robust against supply noise across a wide frequency spectrum.

VI CONCLUSION

The Low Dropout (LDO) voltage regulator plays a vital role in modern electronic systems, particularly where precise voltage regulation and low noise performance are essential. Unlike switching regulators, LDOs offer a simpler design, smaller footprint, and lower output ripple, making them well-suited for sensitive analog, RF, and mixed-signal circuits. Their ability to maintain regulation with a very small difference between input and output voltages (dropout voltage) is especially advantageous in battery-powered and low-voltage applications, where maximizing energy efficiency is critical. Despite lower overall efficiency compared to switching regulators in high current applications, LDOs provide superior performance in scenarios demanding clean power, such as in wearable medical devices, sensors, and portable electronics. Careful design of the error amplifier, compensation techniques (like Miller compensation), and pass element selection ensures stability, fast transient response, and high power supply rejection ratio (PSRR). Thus, the LDO remains an indispensable solution in the design of robust and reliable power management units.

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