Design 2:1 Multiplexer using 16T and 1oT in CMOS Technology

[1]*Prof. Rajesh Kumar Kaushal* , [2]*Anjali M* , [3]*Priya C* , [4]*Roshithashri S* ,
[5]*Vidyasree R*
Department of ECE, Dr. T. Thimmaiah Institute of Technology

Abstract: In this paper, a novel technique presents the design, implementation, and performance analysis of a 2:1 multiplexer using two CMOS-based architectures: a conventional 16-transistor (16T) design and an optimized 10-transistor (10T) design. The objective is to evaluate and compare both implementations in terms of power consumption, speed, and area efficiency under 180nm CMOS technology. The 16T design offers robust noise margins and reliable output drive but at the cost of higher power usage and chip area. In contrast, the 10T design reduces transistor count, achieving lower power consumption (118.28 µW vs. 349.71 µW for 16T) and compact area, while maintaining functional correctness. Simulations conducted using Cadence tools confirm the functional accuracy of both designs and demonstrate the superior energy efficiency of the 10T architecture, making it suitable for low-power and high-density VLSI applications. This comparative study highlights the design trade-offs and provides insights for selecting appropriate MUX implementations in power constrained is used the
environments.

Keywords: CMOSTechnology, 2:1 Multiplexer, Low Power Design, Power Consumption Analysis, 180nm Technology Node.

I. INTRODUCTION

Multiplexers (MUX) play a crucial role in digital circuit design, serving as essential components for data routing, signal selection, and logic synthesis. Among various configurations, a 2:1 multiplexer is one of the simplest and most widely used. It operates by selecting one of two input signals and directing it to the output, based on the logic state of a single control signal.

In modern integrated circuits, the efficiency of multiplexers impacts overall system performance in terms of power consumption, area utilization, and speed. As circuits become denser, reducing power dissipation is vital for portable and battery-operated devices. At the same time, optimizing the number of transistors helps reduce chip area and support miniaturization. Faster signal routing directly contributes to high-speed operations in microprocessors, memory units, and communication systems.

The challenge lies in achieving a balance among these factors. CMOS technology, being the backbone of modern ICs, provides an ideal platform for designing power-efficient and high-performance multiplexers. The use of complementary NMOS and PMOS transistors ensures low static power consumption, high noise immunity, and scalability with shrinking technology nodes.

This paper explores and compares two CMOS-based 2:1 multiplexer designs one using 16 transistors (16T) and the other using 10 transistors (10T) to evaluate trade-offs in performance, power efficiency, and area.

CMOS (Complementary Metal-Oxide-Semiconductor) technology, combining NMOS and PMOS transistors, is widely used due to its low static power dissipation and high noise immunity. Designing efficient multiplexers in CMOS is critical to modern applications in microprocessors, communication systems, and portable devices.

II. LITERATURE SURVEY

A literature survey or a literature review in a project report is that section which shows the various analysis and research made in the field of your interest and the results already published, taking into account that various parameters of the project and the extent of the project. It is the most important part of your report as it gives you a direction in the area of the research. It helps you set a goal for your analysis-thus giving you your problem statement.

Design and Simulation of 2:1 MUX using Various CMOS logic at Different Levels of Technology. The study employs two types of CMOS logic:1. Static CMOS logic,2. Pseudo NMOS logic. The design was implemented using three different technology node scales: 180 nm, 90 nm, and 45 nm. For the 180 nm technology, the results showed a rise time of 1 ns and a fall time of 1 ns, with a leakage power of 2.30 W.For the 90 nm technology, the fall time remained consistent at 1 ns, while the rise time was unspecified. However, the leakage power for this scale also remained the same at 2.30 W. Further details for other parameters, such as rise time for this scale, may need clarification or additional measurement.

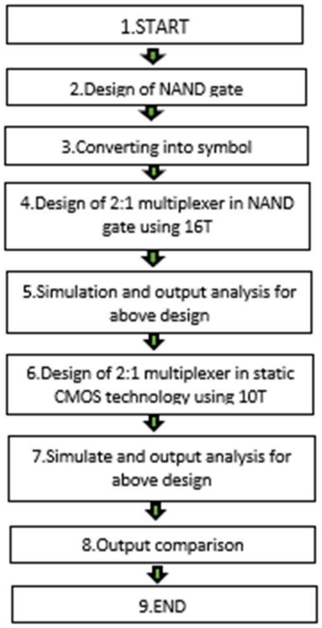
Implementation and Performance Analysis of 2:1 Multiplexer Using Multiple Logic Families at 130 nm Technology. The methodology employed in this study lever agesn CMOS(Complementary Metal-Oxide-Semiconductor) technology, which is widely recognized for its efficiency and versatility in digital circuit design. Specifically, the design is implemented using the 130 nm technology node, a scale that balances performance and power consumption, making it suitable for a range of applications. The results from this implementation highlight two critical performance metrics. First, the power consumption of the circuit is measured at 12.5 W, indicating the energy requirements of the design under operating conditions. Second, the delay observed in the domino logic, a dynamic logic technique often used in high-speed circuits, is found to be 1.2 ns. This delay reflects the speed of signal propagation and the overall performance of the logic implementation. These results provide valuable insights into the efficiency and responsiveness of the CMOS design at the 130 nm technology scale.

Ultra Low Power Multiplexer Design using Variation in CMOS Inverter .The study employed CMOS (Complementary Metal-Oxide-Semiconductor) techniques to design a multiplexer optimized for reduced power consumption and delay. This approach leveraged the inherent advantages of CMOS technology, such as low power dissipation and high performance, to achieve significant improvements in the multiplexer's efficiency. The results of the study demonstrate substantial enhancements in both power and speed. The power consumption of the multiplexer was reduced by 40%, decreasing from 120 µW to 72 µW. Additionally, the delay was minimized by 30%, improving from 10 ns to 7 ns. These reductions highlight the effectiveness of the design methodology in achieving a more energy-efficient and faster multiplexer, making it suitable for applications requiring high performance and low power.

Design and Performance Analysis of 2:1 Multiplexer Using Multiple Logic Families at 180 nm Technology. The study focused on analyzing the performance of a 2:1 multiplexer designed using CMOS logic families at the 180 nm technology node. This methodology emphasized the advantages of CMOS technology, including its efficiency and reliability, to evaluate power consumption and static performance compared to other logic families. The results revealed that the average power consumption of the CMOS multiplexer was 20.06% lower than that of other logic families, demonstrating its superior energy efficiency. Specifically, the designed CMOS multiplexer consumed 12.5 µW of power during operation. In terms of static power consumption, the CMOS logic showed a value of 15.6 µW, which was notably lower compared to 18.2 µW observed in pseudo-NMOS logic. These findings underscore the effectiveness of CMOS logic in achieving low-power designs, making it an ideal choice for energy-sensitive applications.

III. METHODOLOGY

The design methodology for a 2:1 multiplexer in CMOS using both 16T and 10T configurations includes the following steps:



The Methodology section in the file outlines the step-by-step process followed for designing and analysing the 2:1 multiplexer using CMOS technology with both 16-transistor (1f6T) and 10- transistor (10T) implementations. Here's a summary of the key steps:

1. Starting Point:
The design process begins with understanding the requirements and setting up the project framework.

2. Design of NAND Gate:
A NAND gate is designed as a fundamental building block. The NAND gate design is converted into a symbol representation for further use.

3. Design of 2:1 Multiplexer (16T Approach):
The 2:1 multiplexer is designed using the 16-transistor configuration. Simulations are conducted to analyses the output and performance of this design.

4. Design of 2:1 Multiplexer (10T Approach):
The multiplexer is also implemented using a more optimized 10-transistor configuration. Similar simulations and output analyses are performed for this design.

5. Output Comparison:
The results from both the 16T and 10T designs are compared to evaluate performance, power consumption, and area efficiency.

6. Conclusion:
The methodology concludes with a summary of findings and insights gained from the comparison. This structured approach ensures a thorough evaluation of the two design methods, focusing on efficiency and optimization in CMOS technology.

IV. EXPRESSION

The mathematical modeling of CMOS circuits relies on transistor operation equations. In CMOS, NMOS and PMOS operate under three conditions:

1.Cut-off Region: No current flows ($ID = 0$) because $VGS < VTH$.
2. Linear Region**:** The transistor operates as a resistor; $I_D \approx K(V_{GS} - V_{TH})V_{DS} - ½V_{DS}^2$.
3. Saturation Region**:** Transistor acts as a current source; $ID \approx ½K(VGS - VTH)^2$.

These equations are used during transistor sizing and power-delay product calculations.

V. IMPLEMENTATION

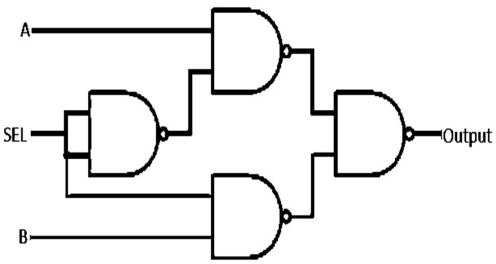


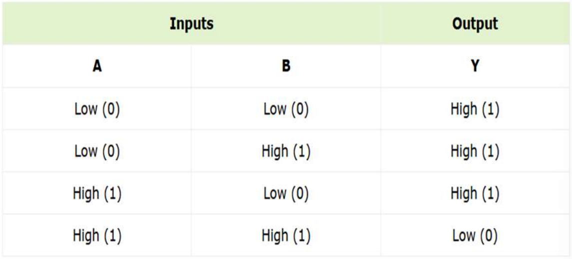
Fig 1 multiplexer using NAND

S	D0	D1	C
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

Table 1 Multiplexer

1. Design of NAND Gate in CMOS:

The NAND gate is a fundamental building block in designing multiplexers and many other digital circuits. A NAND gate is essentially an AND gate combined with a NOT gate, producing an output that is low only when all its inputs are high. In CMOS technology, the design of a NAND gate involves specific arrangements of transistors.



Inputs		Output
A	B	Y
Low (0)	Low (0)	High (1)
Low (0)	High (1)	High (1)
High (1)	Low (0)	High (1)
High (1)	High (1)	Low (0)

Table 2: Truth table for CMOS NAND gate

The NMOS transistors are placed in series, ensuring a conductive path when both inputs are high, resulting in a low output. Conversely, the PMOS transistors are arranged in parallel, allowing the output to be high when either or both inputs are low. This complementary arrangement adheres to the NAND logic.

The design process for a CMOS NAND gate includes several steps. First, the truth table for the NAND gate is verified to ensure its logical operation aligns with the intended output. Following this, the symbol representing the NAND gate is created for schematic representation.
Finally, the design undergoes simulation and waveform analysis to validate its performance, ensuring the output behavior matches the expected logic under varying input conditions. This systematic approach ensures reliable functionality in digital circuits.

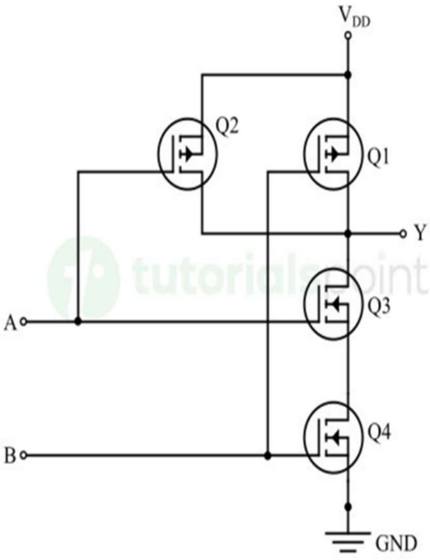


Fig 2: CMOS NAND gate design

2. Implementation of 2:1 Multiplexer (16T and 10T Designs):

A. 16-Transistor (16T) Design

The design incorporates 16 transistors to implement the desired logic equation, effectively achieving the intended functionality with precision. The structure is carefully organized to balance the operation of NMOS and PMOS transistors for complementary behavior.

In operation, the NMOS transistors are responsible for passing the selected data when the control signal is high, ensuring the correct logic flow for active conditions. Conversely, the PMOS transistors take over when the control signal is low, passing the data and maintaining the complementary behavior. This seamless coordination between NMOS and PMOS transistors ensures consistent and accurate performance, aligning with the logic requirements of the circuit.

Steps:

1.Design the multiplexer using the NAND gates and CMOS transistors.
2. Connect input lines (D0, D1) and control signal (S) appropriately.
3. Simulate to verify functionality and generate output waveforms.

B. 10-Transistor (10T) Design:

The optimized design focuses on reducing the number of transistors to improve power efficiency and minimize area usage. By decreasing the component count, the design achieves similar functionality as the 16-transistor (16T) implementation but with a more streamlined and efficient architecture. This reduction not only lowers power consumption but also simplifies the overall complexity of the circuit.

The working principle remains consistent with the 16T design, employing complementary behavior of NMOS and PMOS transistors to achieve the desired logic. However, the optimization lies in reducing redundant transistors, ensuring the design is compact without compromising performance.
The development process involves several steps.
First, the circuit is simplified by identifying and eliminating redundant transistors. Following this, the optimized design is simulated and compared to the 16T implementation to verify its effectiveness. Finally, simulation and output analysis are conducted using Cadence software. This comprehensive tool is employed for designing, simulating, and analyzing the performance of both the optimized and 16T designs, ensuring reliable and accurate results.

Output comparison focuses on metrics like

Power consumption: Lower for the 10T design.
Area efficiency: Better in the 10T design.
Performance:Analysed through waveform outputs for both designs.

IMPLEMENTED NAND GATE :

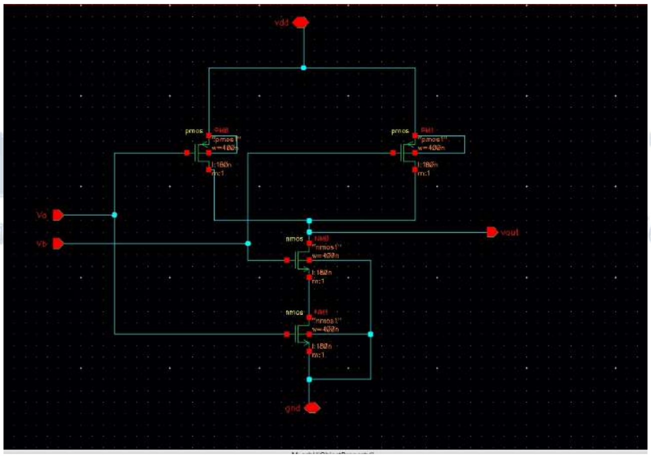


Fig 3 :Implemented NAND Gate in CMOS:

The NAND gate is a fundamental digital logic gate that outputs a low signal (0) only when all its inputs are high (1). The CMOS implementation combines NMOS and PMOS transistors to achieve this behaviour, using their complementary nature.

1. CMOS NAND Gate Design:

Structure: NMOS Transistors: Placed in series. PMOS Transistors: Placed in parallel.
Operation:
When both inputs (A and B) are high (logic 1), the

NMOS path conducts, and the PMOS path is cut off, pulling the output to 0 (logic low), For all other input combinations, at least one PMOS transistor conducts, pulling the output high (logic 1).

2. Symbol of the NAND Gate:

The NAND gate symbol in the file represents a logic block with:
Two inputs: A and B. One output: Y (output of the NAND function).

The symbol visually indicates the logical operation with an AND gate followed by an inversion bubble at the output.

The demo symbol for the implemented NAND gate in CMOS technology represents a simplified, graphical abstraction
Is used for the circuit diagrams and simulations to convey the logic function without detailing the internal transistor arrangements.

IMPLEMENTED NAND GATE DEMO SYMBOL:

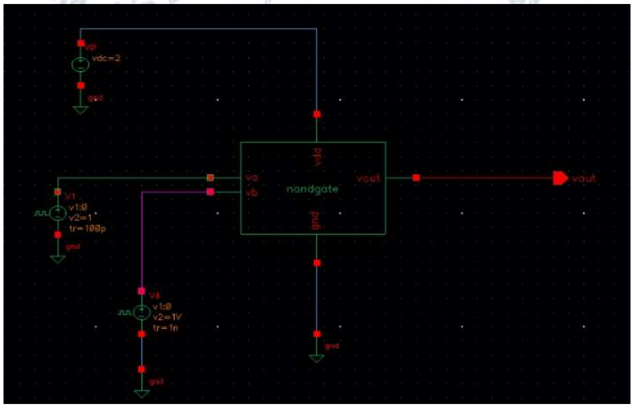


Fig 4 :Implemented NAND Gate Demo Symbol:

Key Features of the Demo Symbol:

1.Graphical Representation:

The symbol represents a NAND gate and incorporates several key features. It consists of two input terminals, which correspond to inputs A and B, and a single output terminal, representing the output Y.

The overall shape of the symbol follows the standard outline of an AND gate, signifying the logical operation at its core. Additionally, a small circle, known as an inversion bubble, is placed at the output terminal. This bubble indicates the negation or NOT operation, which transforms the AND gate into a NAND gate. Together, these elements visually convey the logical functionality of the NAND gate.

2. Purpose: This symbol is used in simulation tools to abstract the physical layout and focus on the logic behaviour. It allows designers to connect this block in larger digital circuits like the 2:1 multiplexer.

NAND GATE SYMBOL:

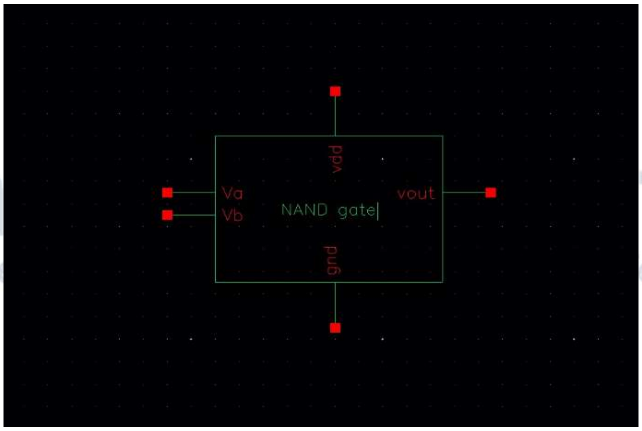


Fig 5: Implementation of NAND Gate symbol

In the context of the NAND gate implementation and simulation in CMOS technology, the following parameters are referenced.

1.Voltage Parameters:

Value	Va	Vb
Voltage 1	0V	0V
Voltage 2	1.8V	1.8V
Period	40ns	20ns
Rise time	100ps	100ps
Fall time	100ps	100ps
Pulse width	20ns	10ns

Table.3:Parameters of NAND Gate Symbol

The variables V1 and V2 represent the input voltages applied to the gate terminals of the transistors within the NAND gate. These inputs correspond to the logical signals fed into the gate for processing. Specifically, V1 is associated with the first input, labeled as A, while V2 corresponds to the second input, labeled as B.

These voltage levels determine the state of the transistors and, consequently, the output behavior of the NAND gate based on its logic operation.

Purpose: These voltage levels determine whether the NMOS and PMOS transistors are in conducting (on) or non-conducting (off) states, thereby controlling the logic output of the gate.

2. Simulation Parameters:

The parameters set in the simulation (e.g., voltage levels, timing of inputs) are critical for generating waveforms and verifying the gate's behaviour. Simulation tools like Cadence were used to configure and analyse these parameters for different input combinations.

3. Output Parameter:

Y (Output): This parameter refers to the output of the NAND gate, determined by the logic: Y=A.B

Significance: These parameters help validate the correct operation of the CMOS NAND gate by testing various input scenarios and measuring the corresponding output response through simulation waveform

RESULT: NAND GATE SYMBOL WAVEFORM:

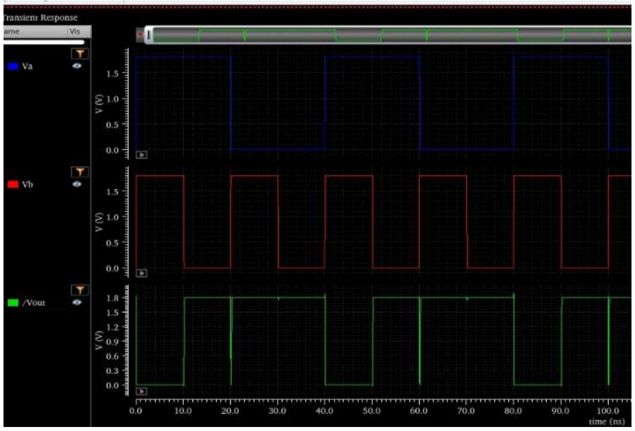


Fig 6:Output waveform of NAND Gate:

IMPLIEMENTATION OF 2:1 MULTIPLEXER USING 16T:

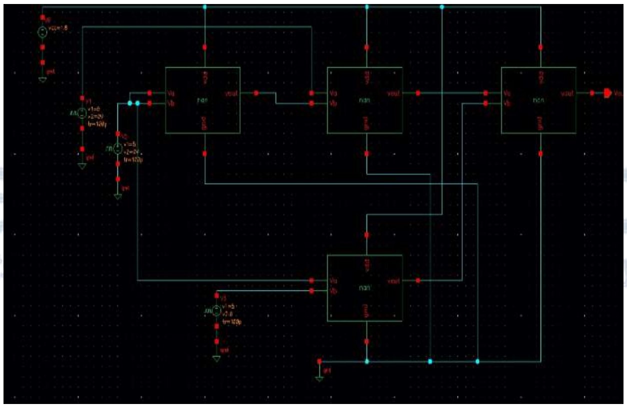


Fig 7: Multiplexer 16T with input and output Parameters

Value	Va	Vb	S
Voltage 1	1.8V	1.8V	1.8V
Voltage 2	0V	0V	0V
Period	40ns	20ns	20ns
Rise time	100ps	100ps	100ps
Fall time	100ps	100ps	100ps
Pulse width	20ns	10ns	10ns

Table 4:Parameters for 2:1 Multiplexer 16T with input and output Parameters

The table provides values for various electrical parameters under different conditions

For Voltage 1, both Va and Vb are set to 1.8V, resulting in an output of 1.8V for S. In Voltage 2, both Va and Vb drop to 0V, which causes the output S to also be 0V.The Period for Va is 40 ns, while Vb and the output S have periods of 20 ns each. The Rise time and Fall time for all three variables Va, Vb, and S are consistently 100 ps, indicating a very fast transition between high and low states. Additionally, the Pulse width is 20 ns for Va , and 10 ns for both Vb and S, reflecting the duration of the high signal in each case.

2:1 MULTIPLEXER 16T INPUT AND OUTPUT WAVEFORM:

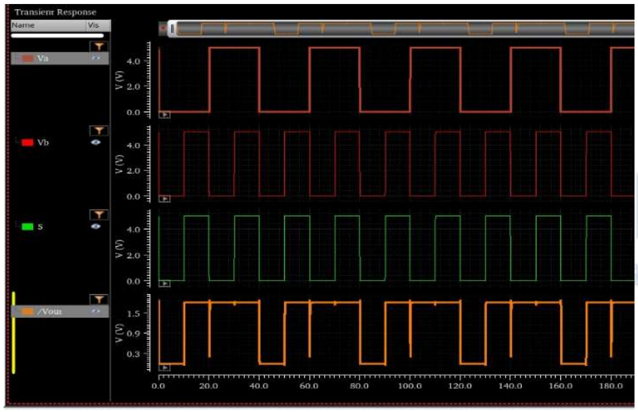


Fig 8: Multiplexer 16T input and output waveform (Transient response)

2:1 MULTIPLEXER USING 16T POWER GRAPH:

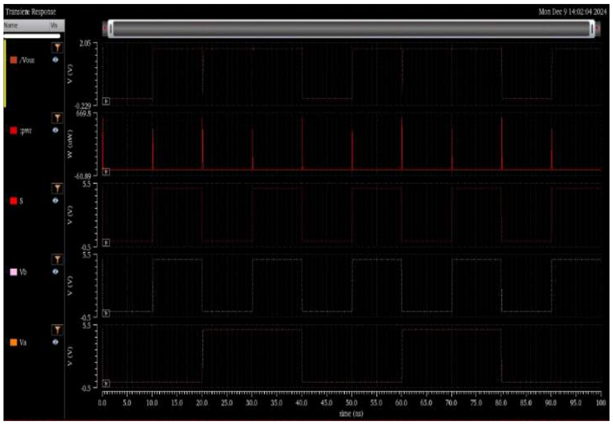


Fig 9: multiplexer using 16t power graph:

The result section summarizes the outcomes of designing, simulating, and analysing the CMOS NAND gate in the project. Here's a detailed breakdown:

Design Validation : The NAND gate was successfully designed and implemented using CMOS technology by combining NMOS and PMOS transistors. This design leverages the complementary nature of these transistors to achieve efficient logical operation with minimal power consumption. The functionality of the NAND gate was verified through its truth table, ensuring correct operation for all possible input combinations.

For inputs A and B, the output Y behaves as follows: when A=0and B=0, the output Y=1; when A=0 and B=1 , the output Y=1; when A=1and B=0, the output Y=1; and finally, when both A=1 and B=1, the output Y=0. This confirms the expected behavior of the NAND gate, where the output is high unless both inputs are high.

2. Simulation and Waveform Analysis: The simulation results were obtained using Cadence software, which generated waveforms showing the behaviour of the NAND gate. The waveforms demonstrated the expected output transitions based on the input voltages (v1 and v2), confirming the gate's functionality.

3. Key Observations:

The output was high (logic 1) for all input combinations except when both inputs were high (logic 1), where the output was low (logic 0), matching the behaviour of a NAND gate.

IMPLIMENTATION OF 2:1 MULTIPLEXER USING 10T:

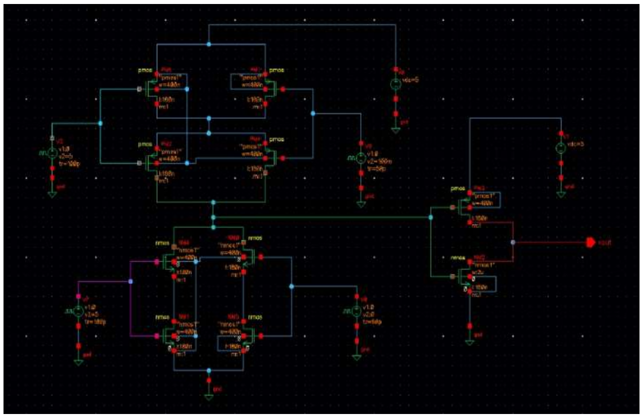


Fig 10: Implimentation of 2:1 multiplexer using 10T

Table: Parameters for 2:1 multiplexer using 10T

Value	Va	Vb
Voltage 1	1.8V	1.8V
Voltage 2	0V	0V
Period	40ns	20ns
Rise time	100ps	100ps
Fall time	100ps	100ps
Pulse width	20ns	10ns

The voltage signals used in the design are characterized by specific parameters to ensure accurate simulation and analysis. Voltage 1 is set to a high level of 1.8V and alternates with a low level of 0V, while Voltage 2 follows the same pattern. The period of the signals is distinct, with Voltage 1 having a period of 40 nanoseconds and Voltage 2 having a shorter period of 20 nano seconds Both signals exhibit fast transition times, with a rise time and fall time of 100 picoseconds each, ensuring sharp transitions between high and low states. The pulse width, representing the duration of the high state, is 20 nanoseconds for Voltage 1 and 10 nanoseconds for Voltage 2. These parameters

are carefully chosen to match the timing requirements and dynamic behavior of the circuit under analysis.

2:1 MULTIPLEXER USING 10T WAVEFORM:

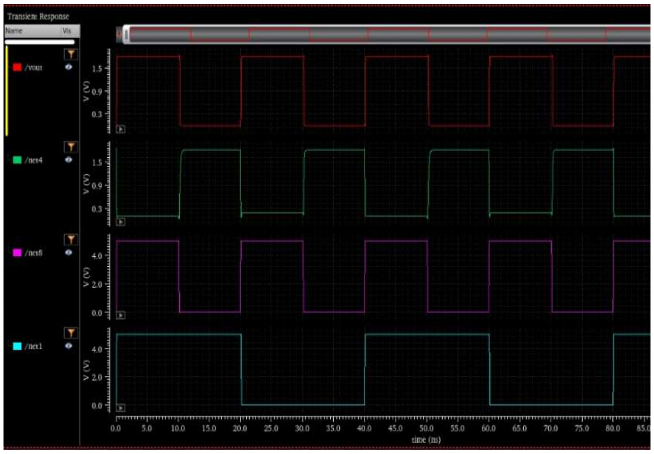


Fig 11: Implimentation of 2:1 multiplexer using 10T

This is typically done using the transient analysis feature in the Cadence simulation environment. During the simulation, the tool records the instantaneous power by multiplying the voltage across the circuit components with the current flowing through them at each time step.

2:1 MULTIPLEXER USING 10T POWER GRAPH

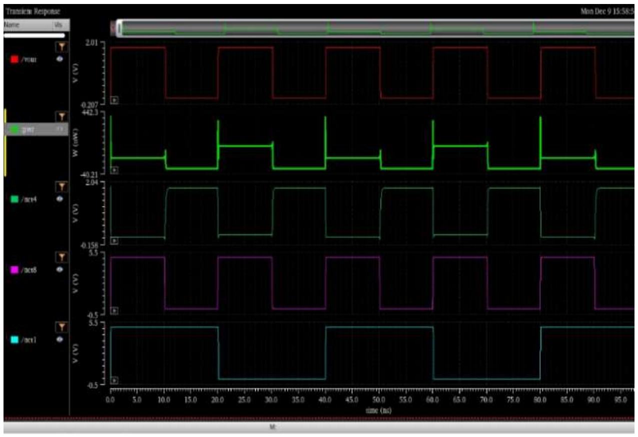


Fig 12 multiplexer using 10T power graph:

The average power is then computed by integrating these instantaneous power values over the total simulation time and dividing by the simulation duration. This method provides an accurate measure of the circuit's power consumption, considering dynamic behavior such as switching activity and steady-state operation. Average power analysis is crucial for optimizing designs to meet low-power requirements, especially in modern CMOS circuits.

The calculation of average power in Cadence involves simulating the circuit under specific operating conditions and analyzing its power consumption over time. This is typically done using the transient analysis feature in the Cadence simulation environment. During the simulation, the tool records the instantaneous power by multiplying the voltage across the circuit components with the current flowing through them at each time step.

The average power is then computed by integrating these instantaneous power values over the total simulation time and dividing by the simulation duration. This method provides an accurate measure of the circuit's power consumption, considering dynamic behavior such as switching activity and steady-state operation. Average power analysis is crucial for optimizing designs to meet low-power requirements, especially in modern CMOS circuits.

VI. RESULT

Output power comparison

Technology used	Average power
2:1 multiplexer using NAND gate(10T) 180nm	$118.28*10^{-6}$ Watt
2:1 multiplexer in static Technology(16T)180nm	$349.711*10^{-6}$ Watt

VII. CONCLUSION

This project successfully presents the design and comparative analysis of a 2:1 multiplexer implemented using 16-transistor (16T) and 10-transistor (10T) CMOS technologies. Multiplexers are fundamental building blocks in digital circuits, and optimizing their performance is critical for efficient VLSI system design. The implementation was carried out using the Cadence software tool with 90nm CMOS technology, enabling detailed simulation and performance analysis.

The 16T multiplexer, built using NAND gate configurations, functions accurately but shows higher power consumption and area requirements due to the increased number of transistors. In contrast, the 10T multiplexer utilizes a static CMOS approach with fewer transistors, resulting in significantly lower power dissipation and reduced chip area. This makes the 10T design more favorable for applications where power and space are critical, such as portable and battery-operated devices or high-density integrated circuits.

Waveform simulations and power graphs clearly demonstrate the superior efficiency of the 10T design compared to its 16T counterpart. The reduction in power and area without compromising functionality proves the effectiveness of minimal transistor design in modern VLSI technology.

Overall, this study highlights the importance of transistor optimization in CMOS logic circuit design. The 10T multiplexer not only achieves the design objective of reducing power, delay, and area but also opens possibilities for its use in high-speed digital applications like encoders and communication systems. This work lays a strong foundation for further advancements in low-power digital design using optimized CMOS logic.

REFERENCES

[1].Adarsh, C. S. D., Lakshmi, T. V., & Kamaraju, M. (2017)

Title: Implementation and comparative analysis of double gate low power multiplexers using dynamic logic styles.

This research was published in the proceedings of the 2017 International Conference of Electronics, Communication, and Aerospace Technology (ICECA). The details of the publication are included in Volume 2 of the conference proceedings. The work can be accessed and referenced using the DOI: 10.1109/ICECA.2017.82128, which provides a direct link to the publication for further review and study.

[2].Vyas, M., Manna, S. K., & Akashe, S. (2015)

Title: Design of power-efficient multiplexer using dual-gate FinFET *technology.*

Published in: 2015 International Conference on Communication Networks (ICCN).

DOI: 10.1109/ICCN.2015.23, providing a reliable reference for further exploration and citation of the study.

[3].D. K. (2015, September)

Title: Ultra-low power multiplexer design using variation in CMOS technology.

Published in: 2015 International Conference on Computer. Communication, and Control (IC4)

DOI: 10.1109/IC4.2015.7357632, which provides a direct link for further access and citation of the study.

[4].Sengupta, P., Banerjee, S., Mitra, S., & Barman, M. (2018)

Title: CMOS Logic Based 2×1 Multiplexer.

This study was published in the proceedings of the 2018 2nd International Conference on Electronics, Materials Engineering & Nano-Technology (IEMENTech). The conference served as a platform for presenting research advancements in electronics, materials engineering, and nano-technology, providing valuable insights into these fields.

[5].Siddhaiah, N., Bhaskar, J. S. B. B., Vidya, B., & Reddy, V. N. (2021

Title: Implementation and Performance Analysis of 2:1 Multiplexer using Different Families at 130nm Technology

This research was published in the proceedings of the 2021 3rd International Conference on Advances in Computing, Communication, Control, and Networking (ICAC3N). The details of the publication can be found on pages 1122 to 1126 of the conference proceedings. For easy access and reference, the work is available through the DOI: 10.1109/ICAC3N.2021.9725706, which provides a direct link to the publication.

[6].C. Jayakumar (2024)

Title: Design of 2:1 Multiplexer using 16T and 10T in a CMOS Technology.

This study was published in the Journal of VLSI Design and Signal Processing, Volume 10, Issue 1. The publication spans pages 10 to 18, providing detailed insights into the research. This journal focuses on advancements in VLSI (Very-Large-Scale Integration) design and signal processing, making it a valuable resource for professionals and researchers in these fields.