Design and Performance Analysis of Full Adder based on Domino Logic Technique

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Abstract: This paper presents the design and performance analysis of a high-speed, low-power full adder circuit using the domino logic technique. Domino logic, known for its superior speed and reduced dynamic power consumption compared to static CMOS logic, is employed to enhance the efficiency of the full adder. The proposed design leverages the inherent advantages of domino logic, such as reduced transistor count and faster operation, while addressing its traditional challenges like charge- sharing and noise sensitivity through optimized circuit techniques. Extensive simulation results demonstrate that the domino-based full adder achieves significant betterment in timing delay and power efficiency in comparison to conventional static CMOS and other dynamic logic designs. The proposed design is particularly well-suited for high-performance arithmetic units in modern microprocessors and digital signal processing applications, offering an effective trade-off between speed, power, and reliability.

Keywords: **Dynamic power consumption, Propagation delay, Charge-sharing**

I.   INTRODUCTION

In the fast-growing VLSI sector, the number of transistors per chip is rising swiftly with every new day. According to Moore's law for every 2 years number of the transistors increases simultaneously delay and power consumption of the device will also increase. To address the need for reduced area and enhanced device performance, an alternative technology is essential. While CMOS technology has been the cornerstone of chip design in the semiconductor industry for decades, the increasing transistor count has led to arise in both device area and delay. Therefore, a transition to a technology with smaller area requirements and reduced delay is necessary. Domino logic has been utilized for designing a one-bit full adder, and its design metrics like area, delay, and power have been evaluated against CMOS technology.

CMOS logic uses p-MOS and n-MOS transistors, which function as pull-up and pull-down components, respectively. When the input is low, the p-MOS transistor activates, charging the output node to Vdd

Conversely, when the input is high, the n-MOS transistor switches on, providing a path to ground and discharging the stored charge at the output node. CMOS logic offers several advantages over earlier technologies, such as a high noise margin, low power consumption, and outputs that cover nearly the full voltage range. However, it also has drawbacks, including the need for a larger area and slower operational speed.

Domino logic is a digital circuit design technique commonly used in high-performance applications such as microprocessors. It is a subset of dynamic logic that operates in two phases: a pre-charge phase, where the output node is charged to a high state, and an evaluate phase, where the logic inputs determine whether the output remains high or discharges to a low state. The name "domino" refers to the unidirectional flow of signals, as each stage triggers the next like falling dominoes. Despite these drawbacks, domino logic is widely used in performance-critical designs such as arithmetic logic units (ALUs) and memory decoders.
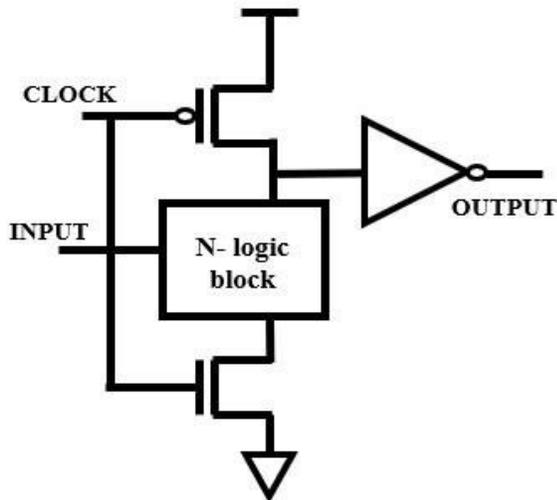
Fig.1.DominoLogic

Domino logic is a high-performance digital circuit design technique that leverages dynamic logic principles to achieve fasters witching speeds and reduced chip area compared to static CMOS circuits. It operates in two distinct clock-driven phases: the pre charge phase, where a PMOS transistor charges the output node to a high state (logic 1), and the evaluate phase, where an NMOS pull-down network processes the input signals to decide whether the output remains high or discharges to a low state (logic 0). The term "domino" reflects the sequential propagation of signals, with the output of one stage triggering the next in a cascading manner, much like falling dominoes. A key feature of domino logic is its unidirectional signal flow, which simplifies timing analysis and prevents feedback issues, making it ideal for high-speed applications. While domino logic offers significant advantages in terms of speed and transistor efficiency, it also introduces challenges such as noise sensitivity, charge sharing, and reliance on precise clock signals. To mitigate these issues, careful design techniques, including the use of inverters and robust clock distribution networks, are employed. Widely used in microprocessors, arithmetic logic units (ALUs), cache memory decoders, and signal processing units, domino logic is a cornerstone of modern high-speed digital circuit design, balancing performance with efficient use of resources.

II. DESIGNING TECHNIQUES

Two design approaches, specifically CMOS logic and domino logic, will be evaluated for building a full adder circuit, and their comparison results will be shown. A full adder is a digital circuit designed to perform binary addition. It is a vital component in the arithmetic and logic units of calculators and computers. The circuit operates with three one- bit inputs, labeled A, B, and C (carry-in), and produces two outputs: the sum and carry-out.
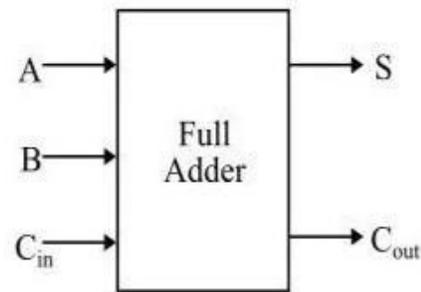

Fig.2.Block diagram of full adder

The logic gate schematic of a single-bit full adder, depicted in Fig.3 employs two XOR gates to produce the sum output, along with two AND gates and one OR gate to derive the carry output. The outputs from the two AND gates are passed into the OR gate, which delivers the carry output of the one-bit full adder.
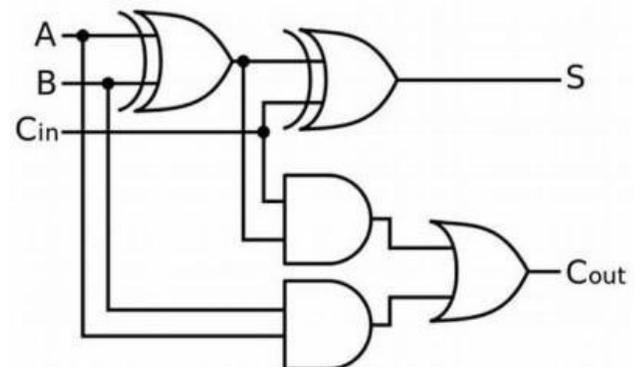

Fig.3.Logic diagram of Full adder

Table I shows the truth table for a full adder constructed using CMOS-based logic which has inputs A, B, Cin and outputs S and Cout. It illustrates all possible input combinations and their

corresponding sum (S) and carry-out (Cout) values, demonstrating the logical behavior of the CMOS-based full adder.

A	B	Cin	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table I. Truth table for Full adder

III. METHODOLOGY

To build a one-bit full adder with domino logic, pMOS transistors are used for the pre-charge stage and inverter, while n-MOS transistors are used for the evaluation phase. This design incorporates 4 p-MOS transistors and 16n-MOS transistors, totaling 20 transistors in the adder circuit. The timing of the pre-charge and evaluation phases is determined by the clock period during simulation. Since domino logic uses fewer transistors, it results in proportional savings in chip area.

IV. EXPRESSION

The circuit's operation is controlled by a clock signal (CLK), which manages the timing and sequence of actions. In Fig.4, the N Logic Block for Carry determines the carry output using the inputs (A, B). This block is connected to a transistor-controlled latch, which manages the timing for storing or transmitting the carry output. The generated inverted carry signal is then processed through a Carry Inverter to restore it to its original form, producing the final carry output, which is subsequently stored.

Similarly, the Sum N Logic Block determines the sum of the input signals. Like the carry logic, the computed sum passes through a transistor-latch-controlled

section to synchronize its operation. Lastly, the sum signal is sent to a Final Inverter for Sum, which guarantees the output is properly inverted to produce the circuit's final sum output. This design ensures precise timing and signal integrity by utilizing transistor-controlled latches and inverters, which are critical for reliable operation in high-speed digital circuits.

$$Carry = AB + BC + AC$$

$$Sum = \overline{ABC} + A\overline{CB} + \overline{BCA} + ABC$$

$$= AB + A\overline{C} + \overline{BC}(C + B + A) + ABC$$

$$= \overline{Carry}\,(C + B + A) + ABC$$

The use of inverter sat the carry and sum outputs ensure that the final output signals meet the required logical polarity, improving compatibility with subsequent digital logic stages. This arrangement enhances the reliability and speed of the circuit, making it suitable for high-performance arithmetic operations in advanced computing systems.
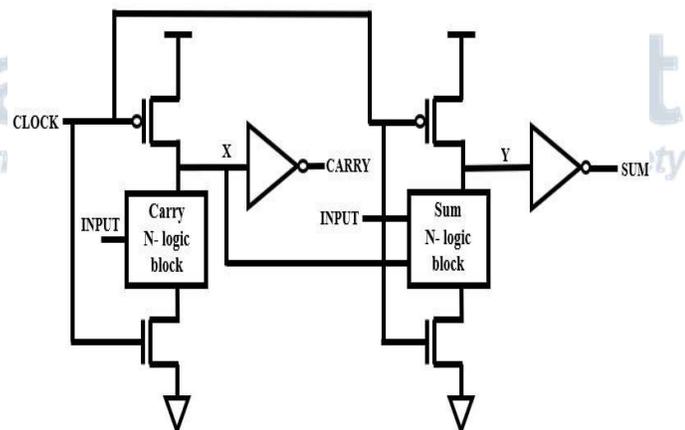

Fig.4. Block Diagram of Full Adder Using Domino Logic

The full adder operates with three inputs: A, B, and Cin. Here, A and B represent the binary digits being added, while Cin serves as the carry input from a previous addition in multi-bit operations. The circuit valuates these inputs using the logic of a full adder, which employs XOR gates to compute the sum and AND/OR gates to determine the carry output. When the clock signal (CLK) is 0, the circuit enters the pre-charge phase, during which the output nodes for sum

and carry are charged to a predefined state in preparation for the next calculation. In this phase, no final outputs are displayed yet. If CLK is 1, the circuit transitions to the evaluation phase, where the actual computation takes place. Following the evaluation, the circuit enters the pre- charge phase again, during which the calculated sum and carry values are finalized and prepared for output. Once these values are ready, they are actively transmitted to the output terminals. The output nodes are driven high, ensuring that the results sum and carry are properly reflected and available for further processing. This clocked operation ensures precise synchronization of the circuit's functions, enabling reliable and efficient computation.
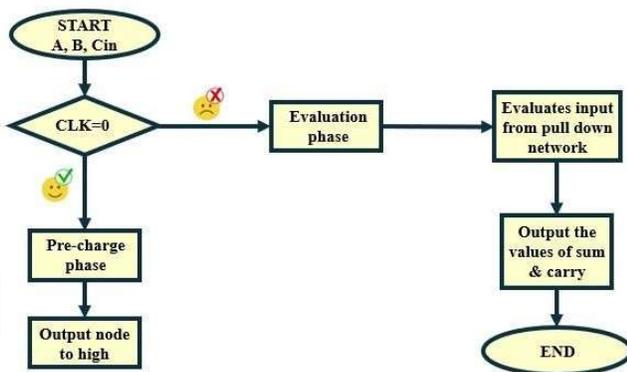

Fig.5.Flowchart of Full Adder Using Domino Logic

V. IMPLEMENTATION

A one-bit full adder based on CMOS logic is illustrated in Fig. 5. This design incorporates 14 p-MOS transistors to charge the output capacitance and 14 n-MOS transistors to discharge the output node depending on the input values. The upper portion of the circuit mainly contains p-MOS transistors responsible for charging the output nodes during logic operations.

Overall, 28 transistors are employed to build a one-bit full adder with CMOS logic. The design method is complex and detailed because of the large number of transistors used. As shown in Fig. 5, the extensive wiring required to interconnect the transistors adds significant complexity and contributes to a
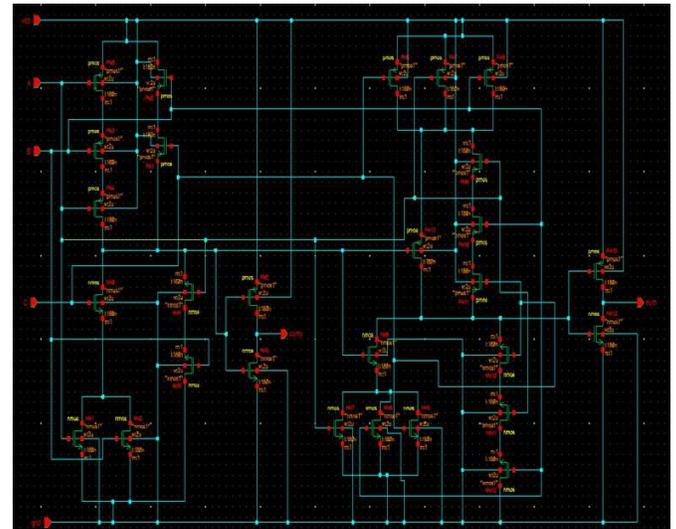
considerable delay in the circuit's operation.

Fig.6.Schematics of Full Adder Using CMOS Logic

The schematic of a one-bit full adder designed using Domino logic is depicted in Fig. 6. This design employs p-MOS transistors for the pre-charge phase and the inverter, while n- MOS transistors are utilized for the evaluation phase. Domino logic uses fewer transistors compared to CMOS logic, making the circuit simpler and faster. It is called "domino" because the operation happens in a sequence, like a chain reaction, where one stage activates the next. This style of circuit is commonly used in high-speed designs, but it requires careful planning to avoid errors like noise and delays.
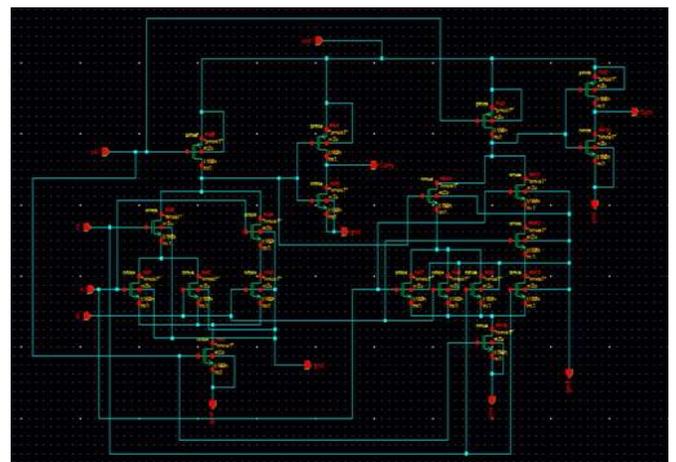

Fig.7.Schematics of Full Adder Using Domino Logic

Specifically, the design incorporates 4 p-MOS transistors and 16 n-MOS transistors, resulting in a total of 20 transistors for constructing the adder circuit using Domino logic.

VI.   RESULT ANALYSIS

The transient response of CMOS and Domino logic circuits was analyzed for 1.8V and 3V operating conditions. The CMOS circuit operating at 1.8V exhibited a transient response of 350ns, with a rise and fall time of 1ps, indicating its ability to switch between logic states quickly and efficiently. In contrast, the CMOS circuit operating at 3V demonstrated a similar transient response of 350ns, but with a rise and fall time of 1ps. The Domino circuit operating at 1.8V and 3V showed a transient response of 350ns, with a rise and fall time of 1ps and 1ps, respectively. This comparison highlights the advantages of CMOS circuits. operating at 1.8V in high-speed applications, while Domino circuits may be more suitable for applications where power consumption is a greater concern.

In CMOS logic, each logic gate requires a separate inverter circuit, which adds to the overall transistor count. In contrast, Domino logic uses a single transistor to implement the logic function and another transistor to pre-charge the output node. This reduces the number of transistors required compared to CMOS logic. Additionally, Domino logic often uses a fewer number of PMOS transistors, which are responsible for pulling the output up to VDD.

The power analysis of the CMOS full adder design, simulated using Cadence, revealed a power consumption of 7.563mW for the 1.8V design and 29.896mW for the 3V design. The delay analysis showed that the 1.8V design exhibited a delay of 30.19ns, while the 3V design showed a delay of 30.16ns. The power analysis of the full adder using domino logic design, simulated using Cadence, revealed a power consumption of 2.667mW for the 1.8V design and 9.070mW for the 3V design. The delay analysis showed that the 1.8Vdesign exhibited a delay of 77.64ps, while the 3V design showed a

delay of 54.48ps According to delay theory, the delay of a digital circuit is directly proportional to the RC time constant, which is influenced by the transistor size, wire resistance, and capacitance. Therefore, optimizing transistor size and wire routing can significantly reduce delay and improve overall circuit performance.

Fig 8. Power Analysis of Full Adder Using CMOS Logic with 3V
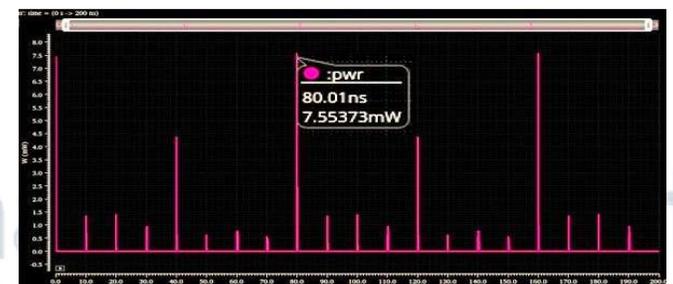

Fig 9. Power Analysis of Full Adder Using CMOS Logic with 1.8V

A comparative analysis of two full adder circuits using Domino logic in Cadence Virtuoso was performed, with the primary difference being the supply voltage. The first circuit, operating at a supply voltage of 1.8V, exhibited a settling time of 350 nanoseconds (ns) in its transient response analysis, indicating are liable and stable output. The power analysis results showed a total power consumption of 2.667 milli watts(mW), with a rise time and fall time of 0.9 ns. The propagation delay of this circuit was measured to be 77.64 picoseconds (ps) or 77.64 x 10^-12 seconds. In contrast, the second circuit, operating at a supply voltage of 3V, exhibited a settling time of 350ns in its transient response analysis, similar to the first circuit. However, the power analysis results showed a significantly higher total power consumption of 9.070 mW. The rise time and fall time

of this circuit were measured to be1.5 ns, which is significantly higher than the first circuit. On the other hand, the propagation delay of this circuit was measured to be 54.48 ps or 54.48 x 10^-12 seconds, which is lower than the first circuit.
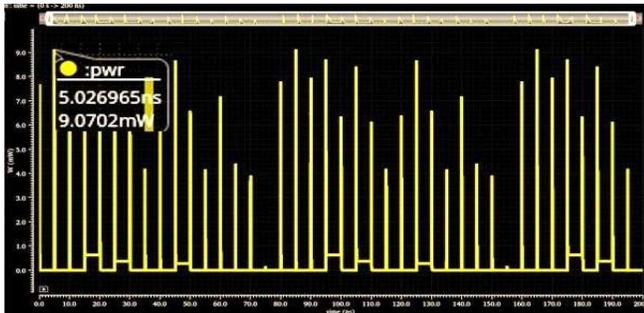
POWER	CMOS LOGIC	DOMINO LOGIC
1.8 V	7.553 mW	2.267 mW
3 V	29.896 mW	9.070 mW

Table 2.Comparison of Power Analysis

Fig.10. Power Analysis of Full Adder Using Domino Logic with 3V

DELAY	CMOS LOGIC	DOMINO LOGIC
1.8 V	30.19 ns	77.64 ps
3 V	30.16 ns	54.48 ps

Table 3.Comparison of Delay

Fig.11. Power Analysis of Full Adder Using Domino Logic with 1.8V

VII.   CONCLUSION

The full adder based on Domino logic has been created and simulated using Cadence Virtuoso design tools with 180 nm technology. The results have consistently demonstrated the superiority of Domino logic circuits in terms of power consumption and propagation delay. The CMOS full adder circuit, operating at a supply voltage of 1.8V and 3V, exhibited a settling time of 350 nanoseconds (ns) in its transient response analysis, consuming power measured at 7.563 milliwatts (mW) for 1.8V and 29.896milliwatts (mW), a propagation delay of 30.19 nanoseconds (ns) and 30.16 nanoseconds (ns) .In contrast, the Domino logic full adder circuit, operating at a supply voltage of 1.8Vand 3V, exhibited a settling time of 350 ns in its transient response analysis, with a significantly lower power consumption of 2.667 mW for 1.8V and 9.070 milliwatts (mW) for 3V and a faster propagation delay of 77.64 picoseconds (ps) for 1.8V and 54.48 picoseconds (ps) for 3V. The effect of supply voltage on the performance of Domino logic full adder circuits was examined. Results indicated that raising the supply voltage from 1.8V to 3V caused a notable rise in power usage, but also decreased propagation delay. These findings are crucial for improving the design of efficient, low-power digital circuits. Using Domino logic circuits can greatly reduce power consumption, making them well-suited for battery-operated devices and other energy-saving applications. Additionally, the fast propagation delay

Fig.12. Delay of Full Adder Using CMOS Logic with 1.8V and 3V

Fig.13. Delay of Full Adder Using Domino Logic with 1.8V and 3V

of Domino logic circuits makes them suitable for high-speed digital applications.

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